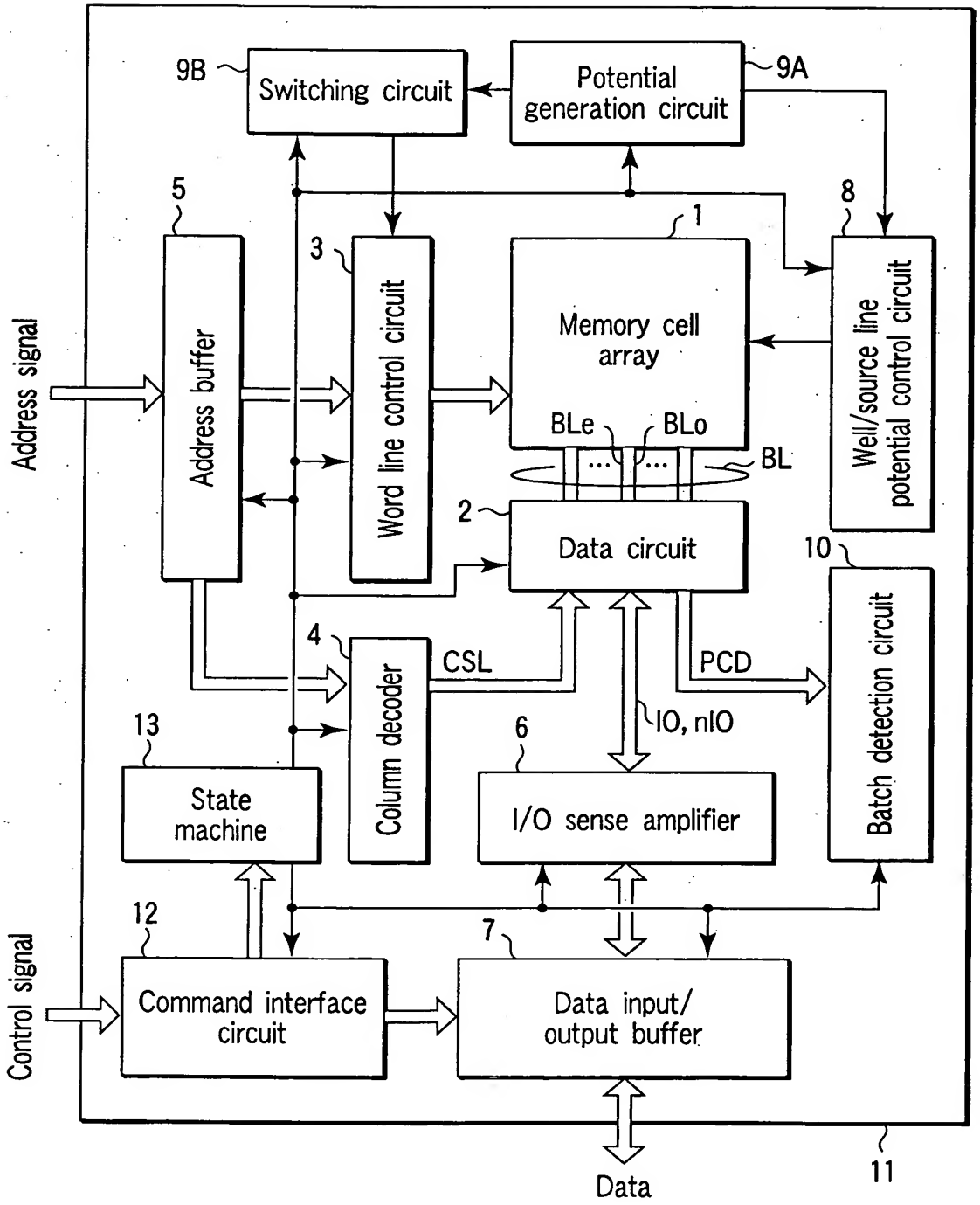

9B
Switching circuit
Potential generation circuit
9A
5
8
1
3
Address signal
Address buffer
Word line control circuit
Memory cell array
Well/source line potential control circuit
BLe
BLo
BL
2
Data circuit
10
4
CSL
PCD
Column decoder
IO, nIO
Batch detection circuit
13
6
State machine
I/O sense amplifier
12
7
Control signal
Command interface circuit
Data input/ output buffer
Data
11

FIG. 1

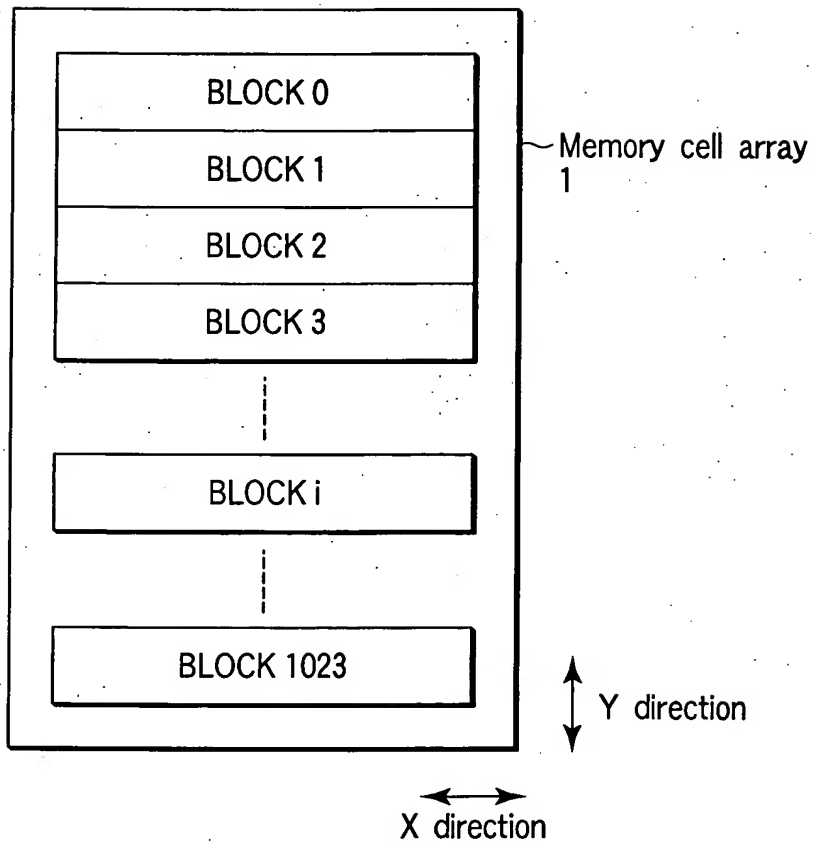

BLOCK 0
BLOCK 1
BLOCK 2
BLOCK 3
BLOCK i
BLOCK 1023
Memory cell array 1
Y direction
X direction

FIG. 2

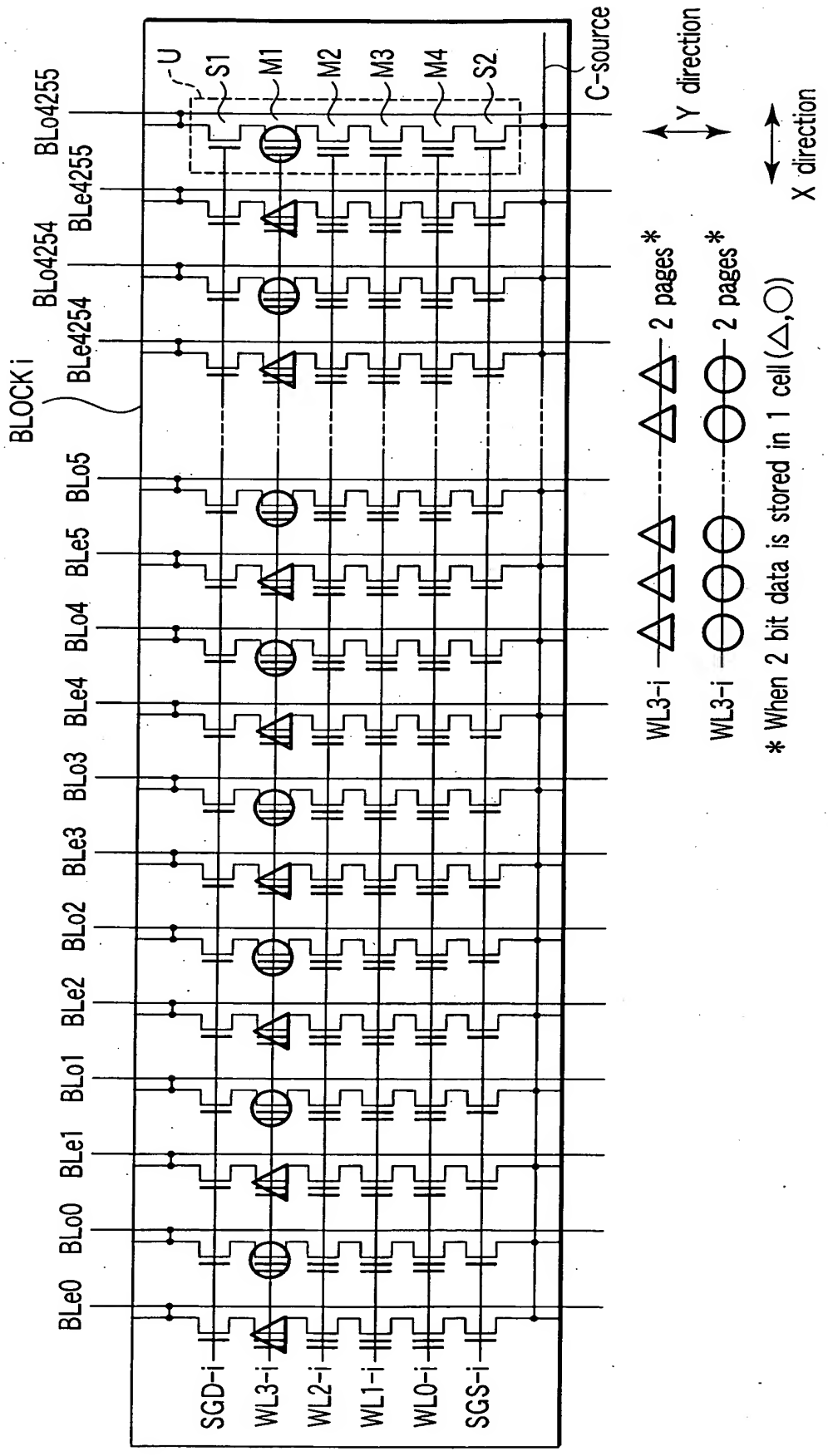

BLOCK i
U
S1
M1
M2
M3
M4
S2
C-source
BLo4255
BLe4255
BLo4254
BLe4254
BLo5
BLe5
BLo4
BLe4
BLo3
BLe3
BLo2
BLe2
BLo1
BLe1
BLo0
BLe0
SGD-i
WL3-i
WL2-i
WL1-i
WL0-i
SGS-i
Y direction
X direction
WL3-i
2 pages*
WL3-i
2 pages*
* When 2 bit data is stored in 1 cell (△,○)

FIG. 3

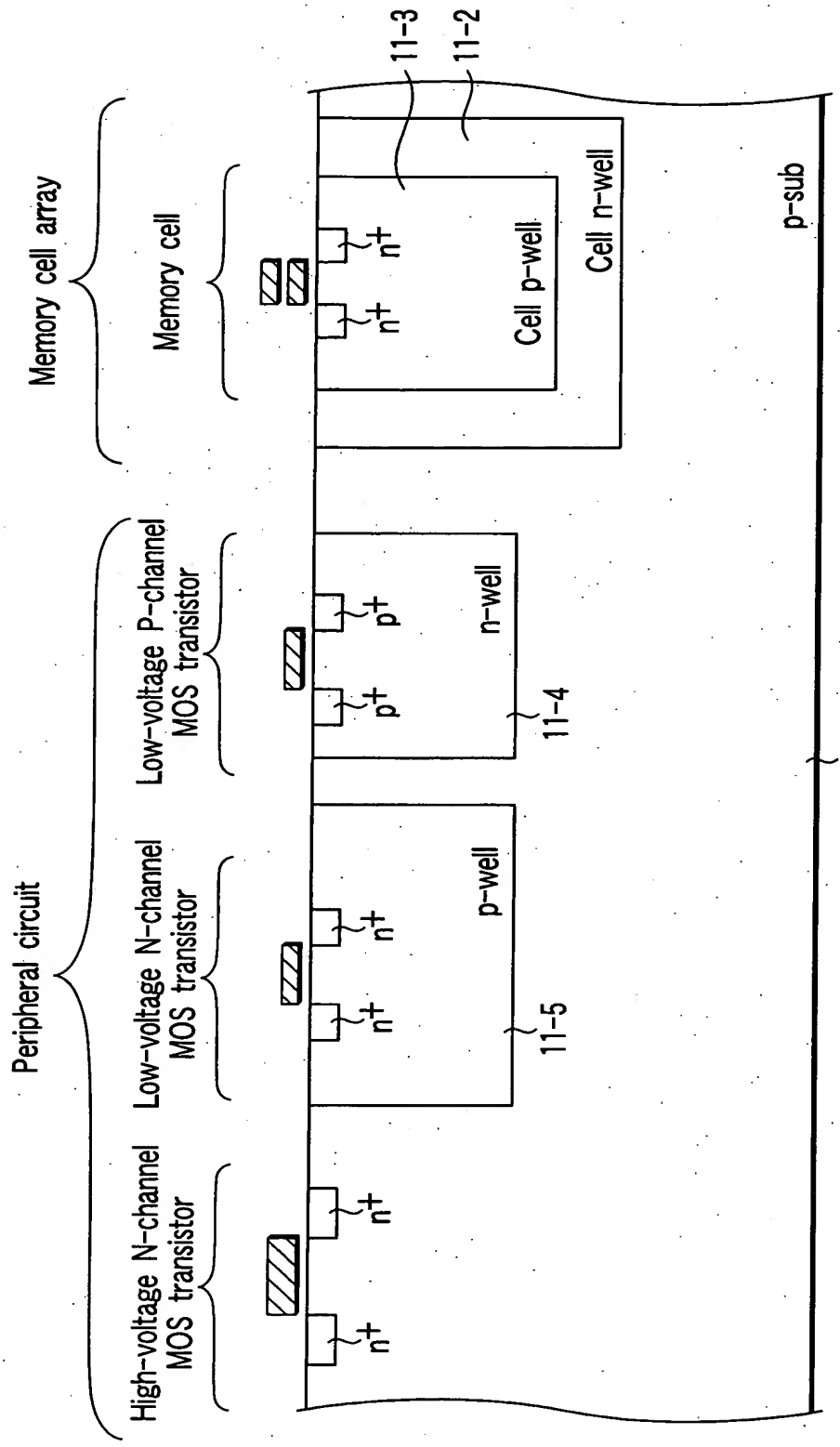

Memory cell array
Memory cell
Peripheral circuit
Low-voltage P-channel MOS transistor
Low-voltage N-channel MOS transistor
High-voltage N-channel MOS transistor
n+
p+
Cell p-well
Cell n-well
n-well
p-well
p-sub
11-1
11-2
11-3
11-4
11-5

FIG. 4

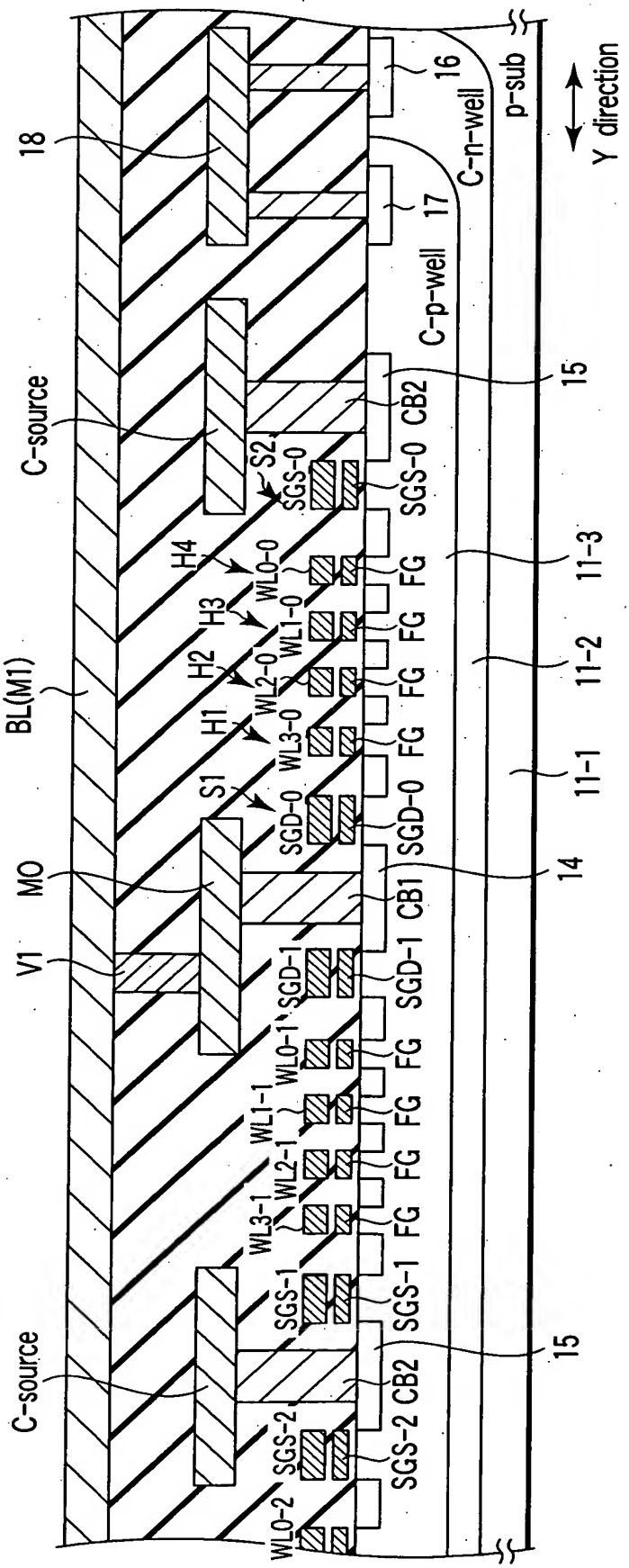

C-source
BL(M1)
V1
MO
C-source
18
16
17
15
15
14
C-n-well
C-p-well
p-sub
Y direction
11-3
11-2
11-1
CB2
CB1
CB2
SGS-0
SGS-1
SGS-2
SGD-0
SGD-1
FG
H4
H3
H2
H1
S2
S1
WL0-0
WL1-0
WL2-0
WL3-0
WL0-1
WL1-1
WL2-1
WL3-1
WL0-2

FIG.5

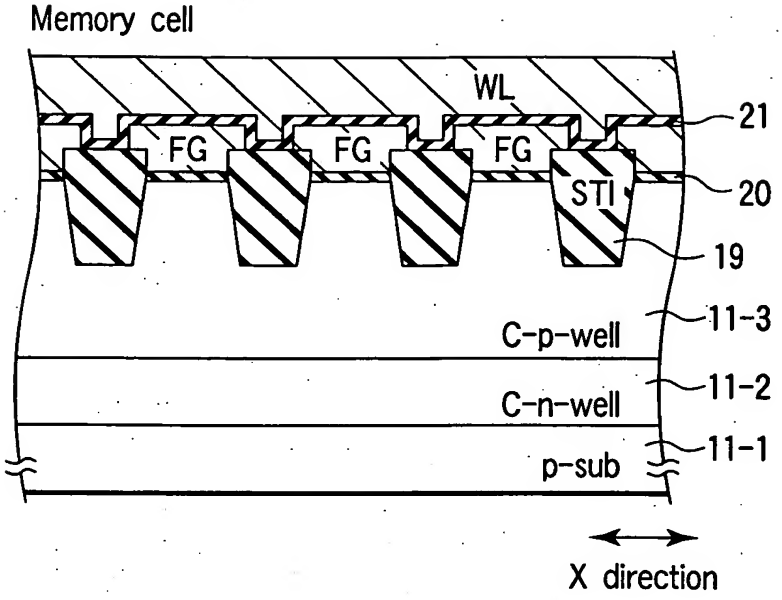

Memory cell
WL
21
FG
FG
FG
STI
20
19
11-3
C-p-well
11-2
C-n-well
11-1
p-sub
X direction

FIG. 6

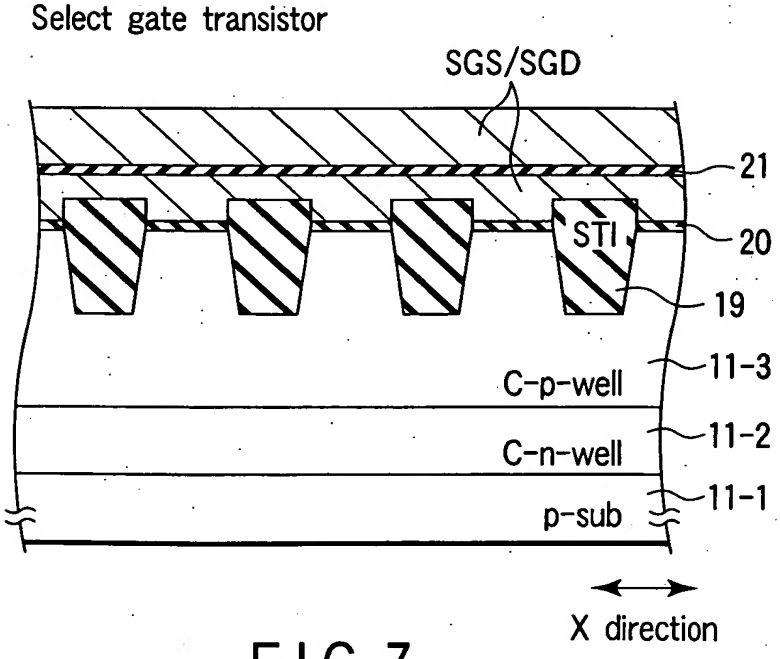

Select gate transistor
SGS/SGD
21
STI
20
19
11-3
C-p-well
11-2
C-n-well
11-1
p-sub
X direction

FIG. 7

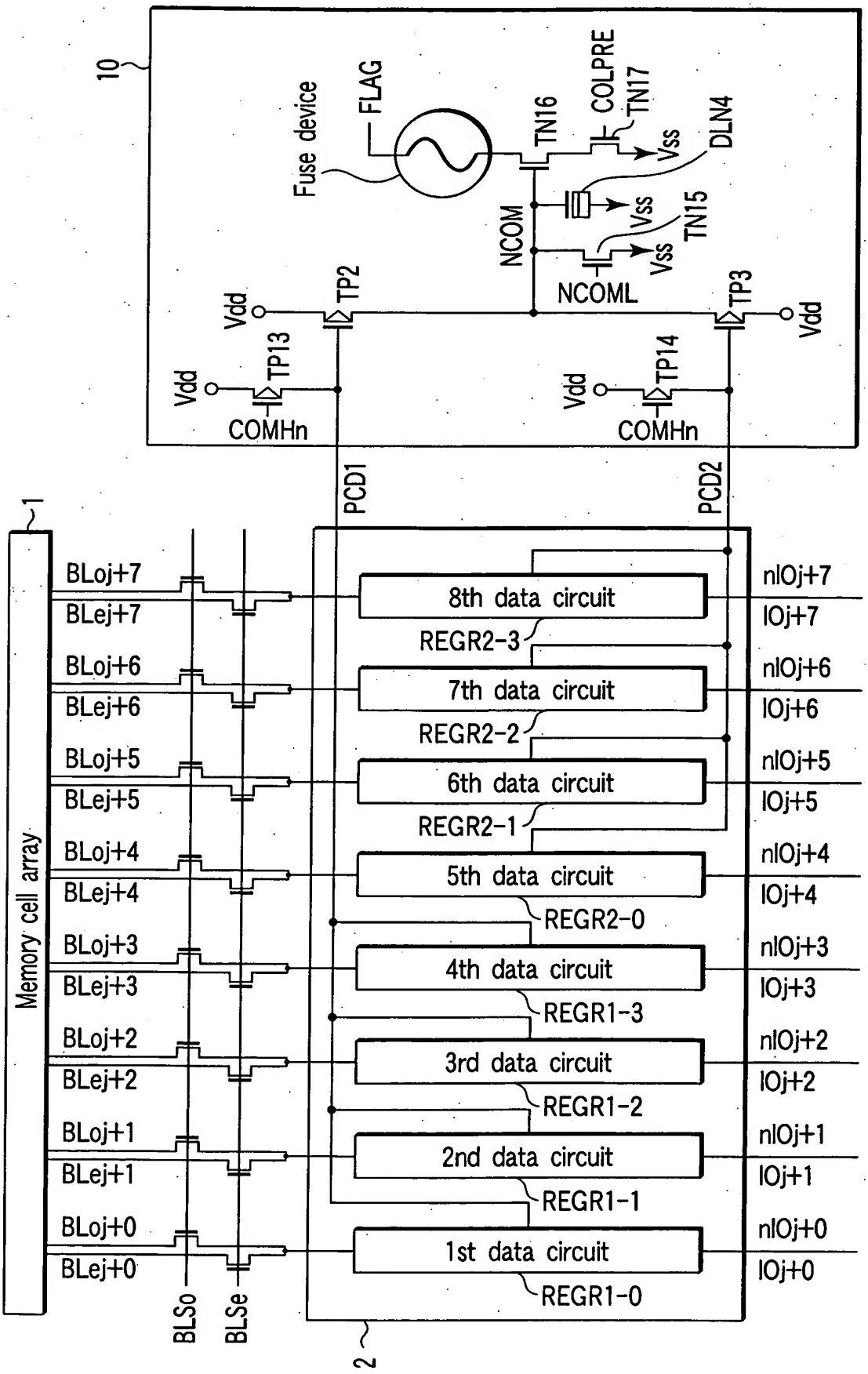

10
Fuse device
FLAG
TN16
COLPRE
TN17
Vss
DLN4
NCOM
Vss
TN15
Vss
NCOML
Vdd
TP2
TP3
Vdd
Vdd
TP13
COMHn
Vdd
TP14
COMHn
PCD1
PCD2
1
Memory cell array
BLoj+7
BLej+7
BLoj+6
BLej+6
BLoj+5
BLej+5
BLoj+4
BLej+4
BLoj+3
BLej+3
BLoj+2
BLej+2
BLoj+1
BLej+1
BLoj+0
BLej+0
BLSo
BLSe
8th data circuit
7th data circuit
6th data circuit
5th data circuit
4th data circuit
3rd data circuit
2nd data circuit
1st data circuit
REGR2-3
REGR2-2
REGR2-1
REGR2-0
REGR1-3
REGR1-2
REGR1-1
REGR1-0
nIOj+7
IOj+7
nIOj+6
IOj+6
nIOj+5
IOj+5
nIOj+4
IOj+4
nIOj+3
IOj+3
nIOj+2
IOj+2
nIOj+1
IOj+1
nIOj+0
IOj+0
2

FIG. 8

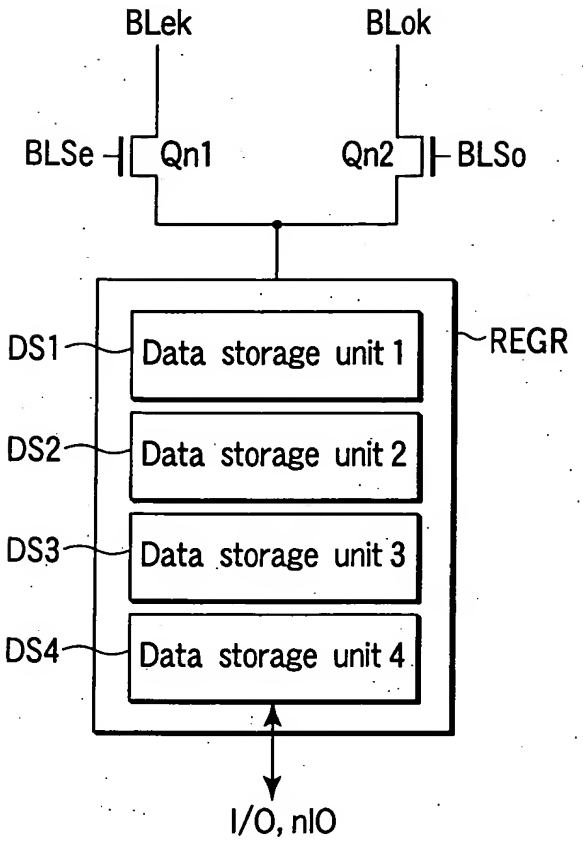

BLek
BLok
BLSe
Qn1
Qn2
BLSo
DS1
Data storage unit 1
REGR
DS2
Data storage unit 2
DS3
Data storage unit 3
DS4
Data storage unit 4
I/O, nIO

FIG. 9

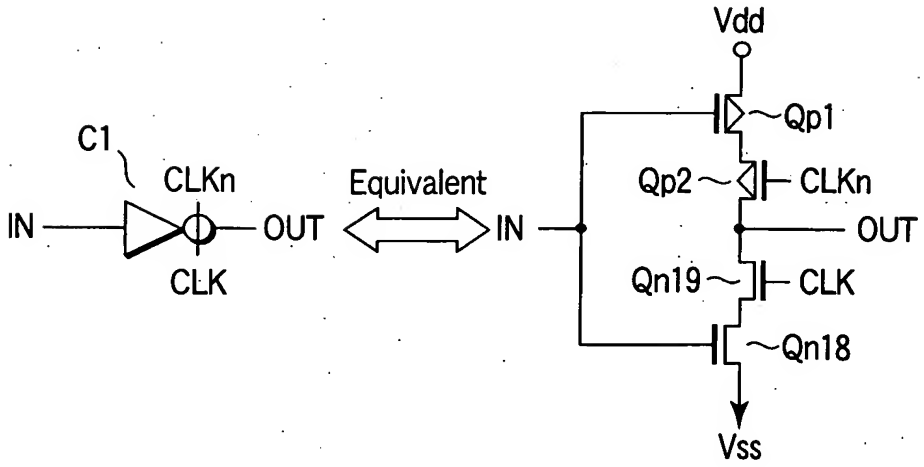

Vdd
C1
CLKn
IN
OUT
CLK
Equivalent
IN
Qp1
Qp2
CLKn
OUT
Qn19
CLK
Qn18
Vss

FIG. 11

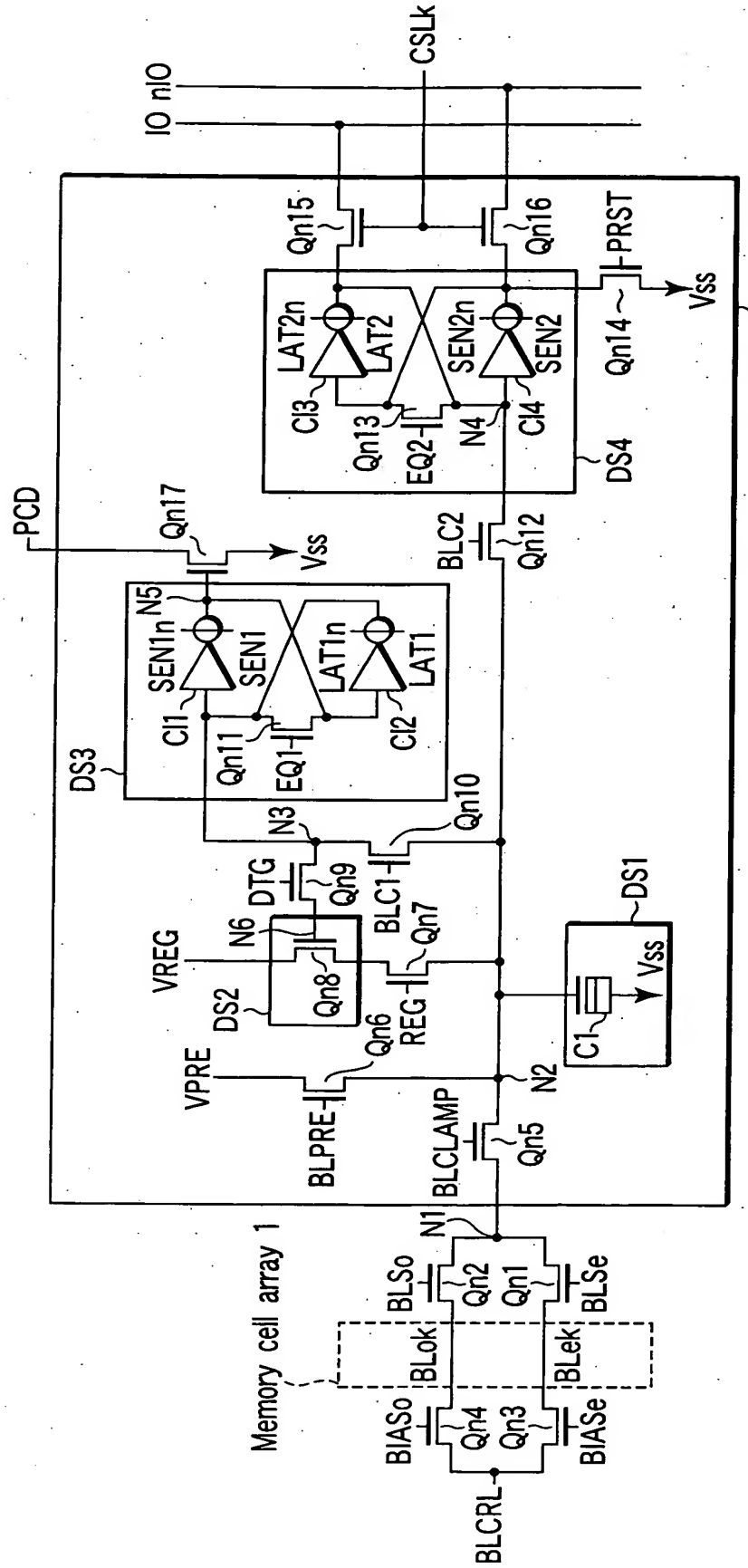
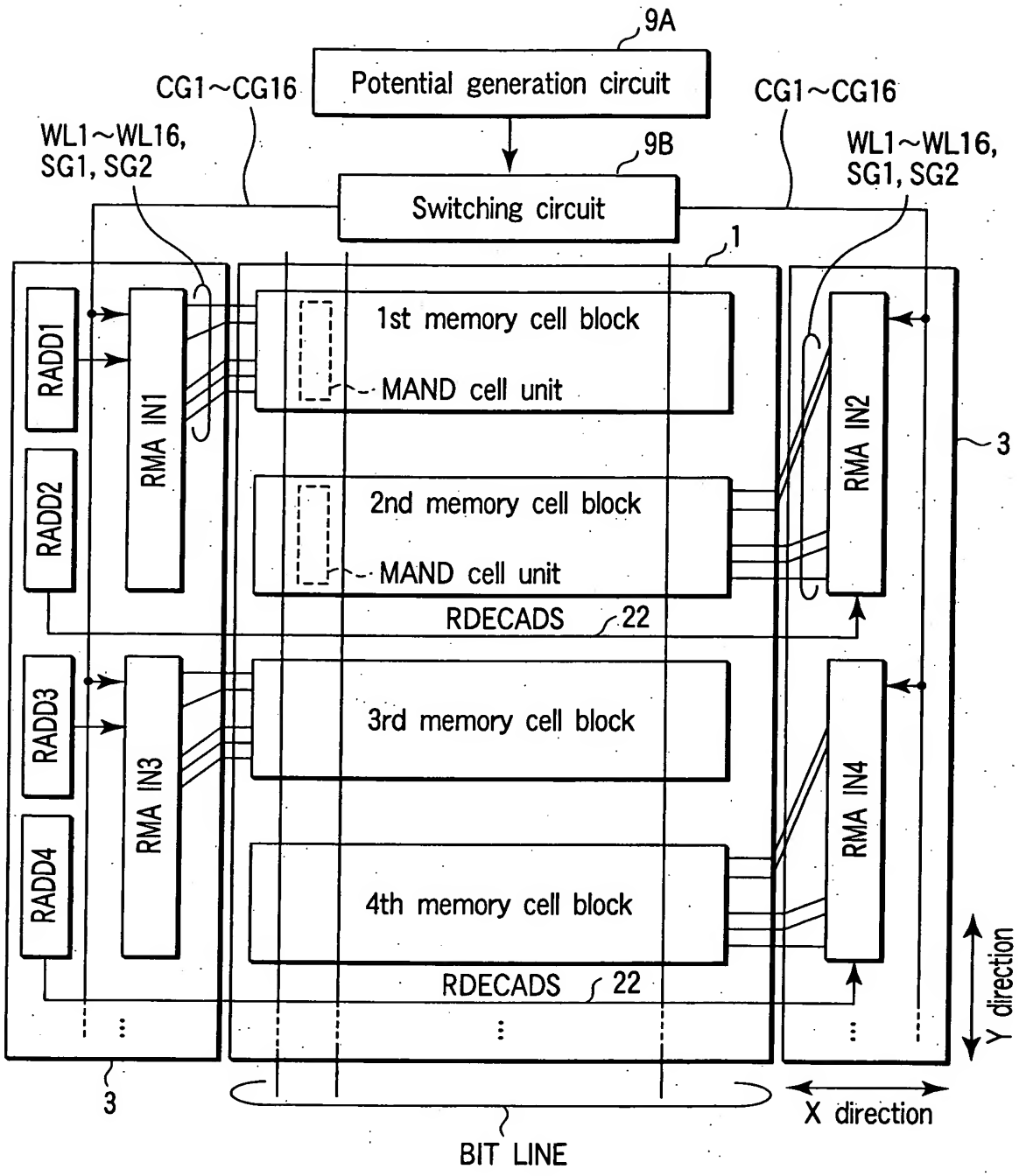

IO nIO
CSLk
Qn15
Qn16
PRST
Vss
REGR
LAT2n
LAT2
SEN2n
SEN2
Qn14
CI3
Qn13
EQ2
N4
CI4
DS4
PCD
Qn17
Vss
BLC2
Qn12
N5
SEN1n
SEN1
LAT1n
LAT1
CI1
Qn11
EQ1
CI2
DS3
N3
Qn10
DTG
Qn9
BLC1
Qn7
DS1
VREG
N6
Qn8
DS2
Qn6
REG
Vss
C1
VPRE
BLPRE
BLCLAMP
Qn5
N2
N1
Memory cell array 1
BLSo
Qn2
Qn1
BLSe
BLok
BLek
BIASo
Qn4
Qn3
BIASe
BLCRL

FIG. 10



RMAINi : i-th word line driver
RADDi : i-th row address decoder
RDECADS : Word line driver selection signal
i=1, 2, 3, 4, ···

FIG. 12

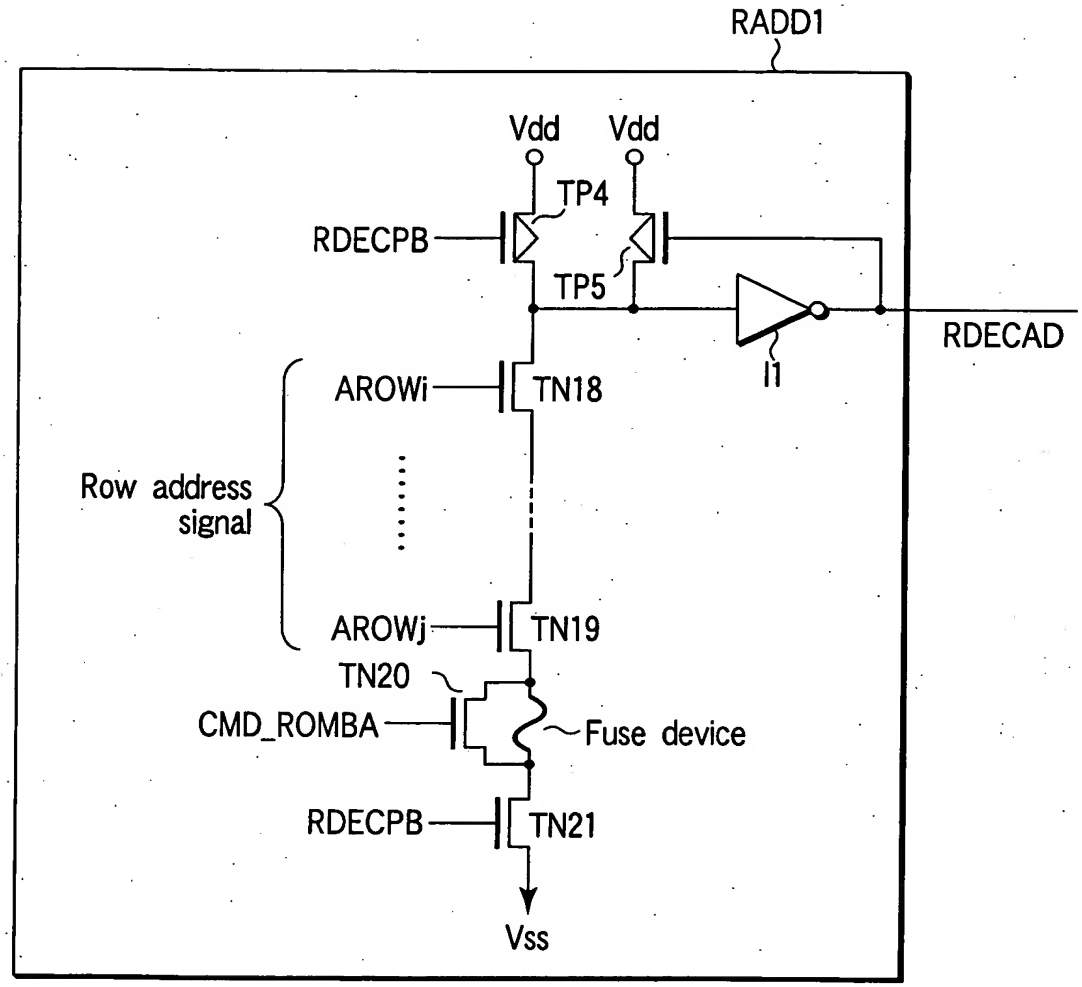

RADD1
Vdd
Vdd
TP4
RDECPB
TP5
RDECAD
I1
AROWi
TN18
Row address signal
AROWj
TN19
TN20
CMD_ROMBA
Fuse device
RDECPB
TN21
Vss

FIG. 13

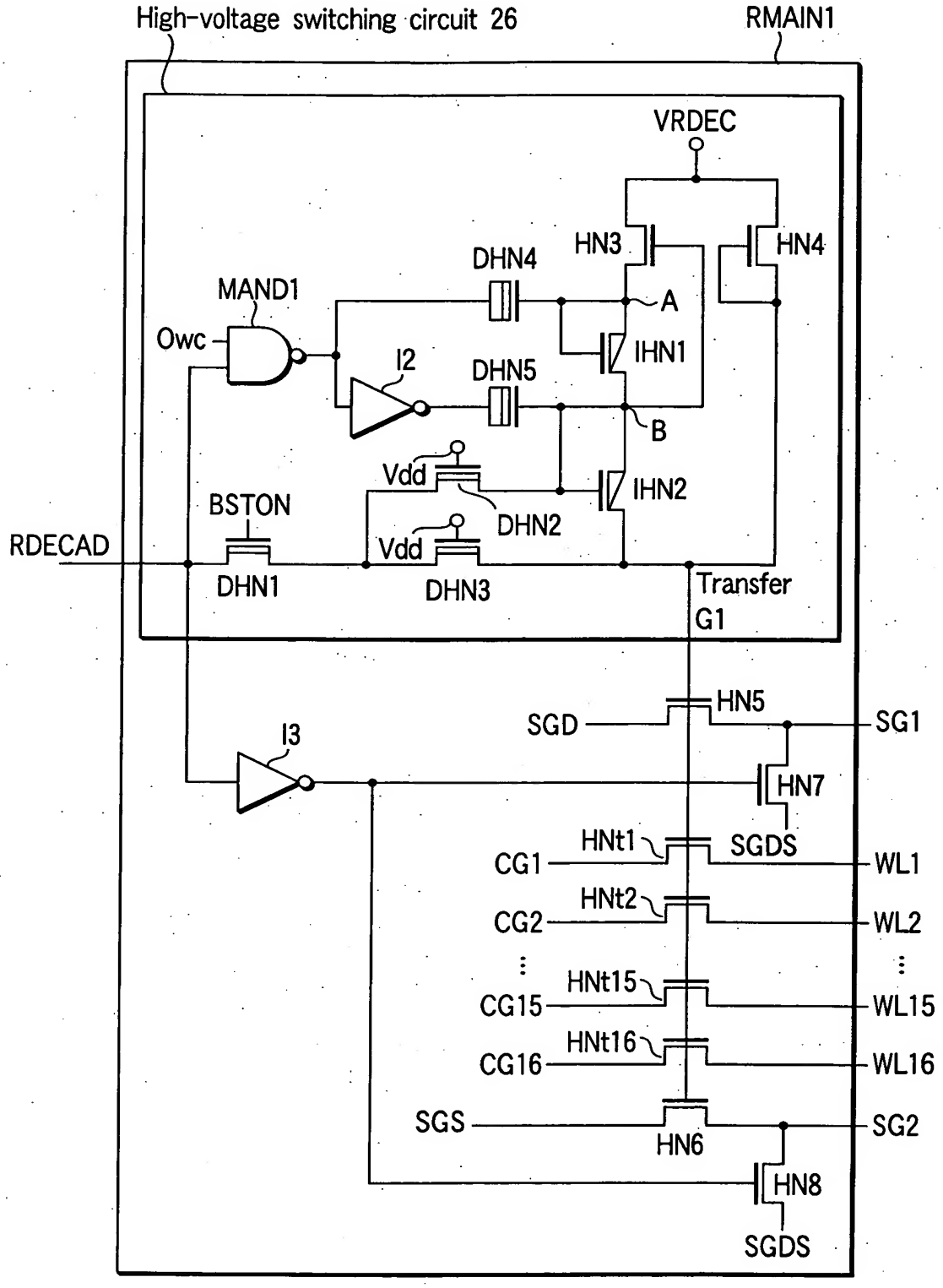

High-voltage switching circuit 26
RMAIN1
VRDEC
HN3
HN4
DHN4
MAND1
A
Owc
IHN1
I2
DHN5
B
Vdd
IHN2
BSTON
DHN2
RDECAD
Vdd
DHN1
DHN3
Transfer G1
HN5
SGD
SG1
I3
HN7
HNt1
SGDS
CG1
WL1
HNt2
CG2
WL2
HNt15
CG15
WL15
HNt16
CG16
WL16
SGS
HN6
SG2
HN8
SGDS

FIG. 14

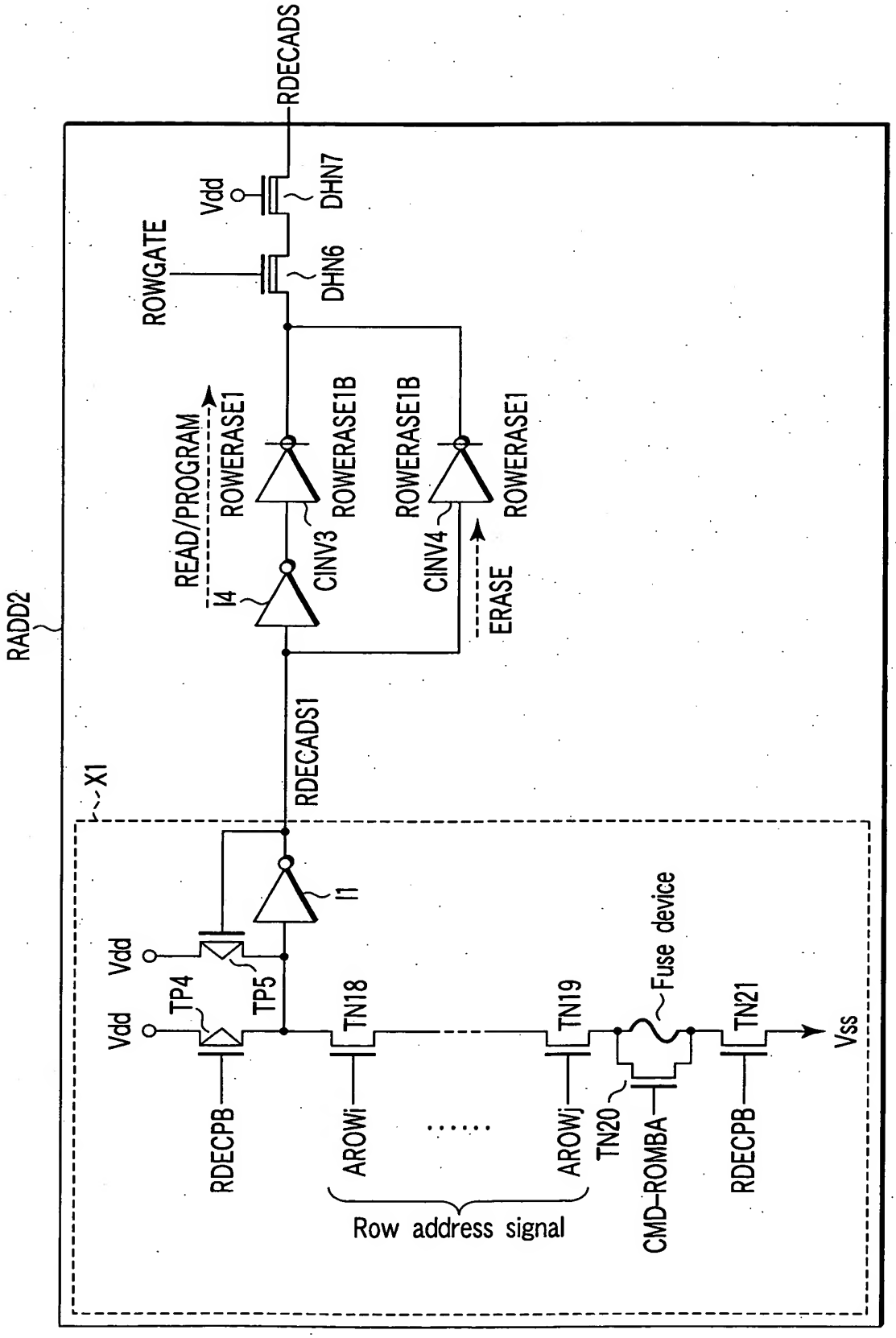

RDECADS
Vdd
DHN7
ROWGATE
DHN6
READ/PROGRAM
ROWERASE1
ROWERASE1B
ROWERASE1B
ROWERASE1
RADD2
I4
CINV3
CINV4
ERASE
RDECADS1
X1
I1
Vdd
Vdd
TP4
TP5
TN18
TN19
Fuse device
TN21
Vss
RDECPB
AROWi
AROWj
TN20
CMD-ROMBA
RDECPB
Row address signal

FIG. 15

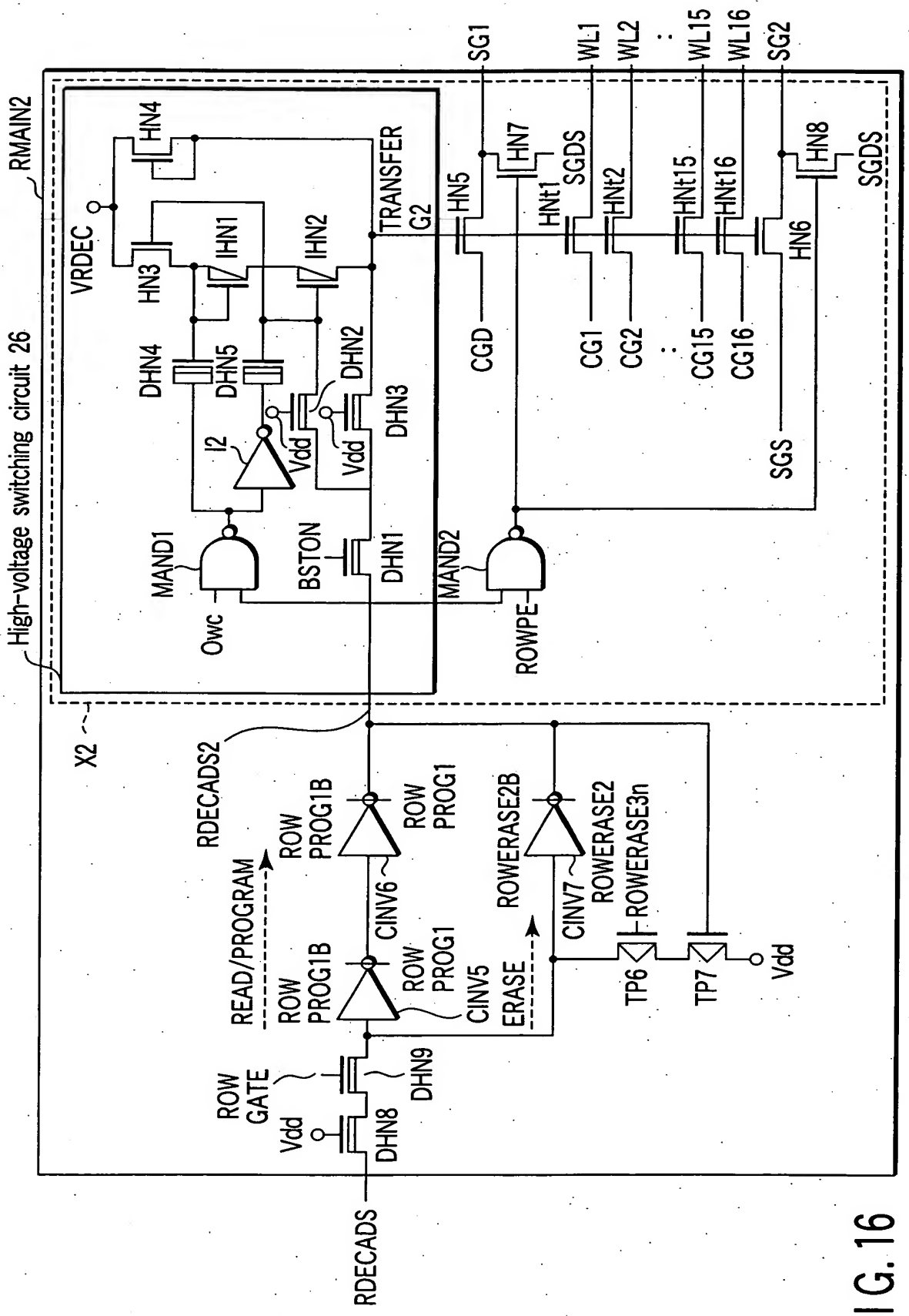

RMAIN2
High-voltage switching circuit 26
X2
VRDEC
HN4
HN3
IHN1
IHN2
DHN4
DHN5
DHN2
DHN3
I2
Vdd
MAND1
Owc
BSTON
DHN1
TRANSFER G2
MAND2
ROWPE
SG1
WL1
WL2
WL15
WL16
SG2
HN5
HN7
HNt1
SGDS
HNt2
HNt15
HNt16
HN6
HN8
CGD
CG1
CG2
CG15
CG16
SGS
RDECADS2
ROW PROG1B
ROW PROG1
READ/PROGRAM
CINV6
CINV5
ERASE
ROWERASE2B
ROWERASE2
ROWERASE3n
CINV7
TP6
TP7
ROW GATE
DHN9
DHN8
RDECADS

FIG. 16

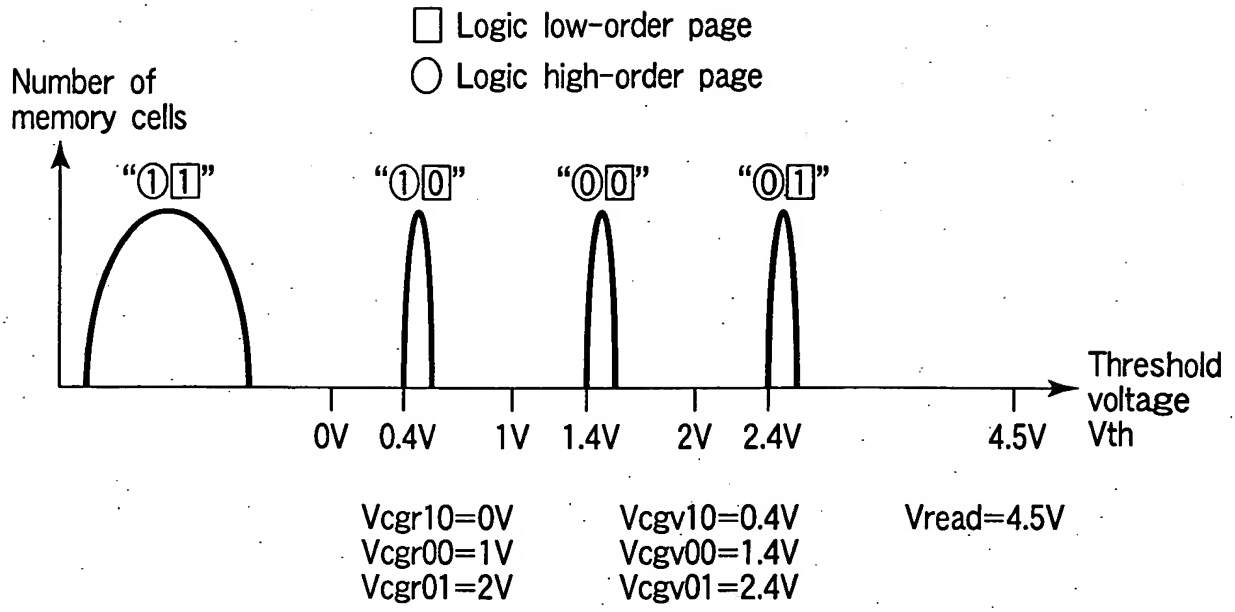

Logic low-order page
Logic high-order page
Number of memory cells
"11"
"10"
"00"
"01"
Threshold voltage Vth
0V
0.4V
1V
1.4V
2V
2.4V
4.5V
Vcgr10=0V
Vcgr00=1V
Vcgr01=2V
Vcgv10=0.4V
Vcgv00=1.4V
Vcgv01=2.4V
Vread=4.5V

FIG. 17

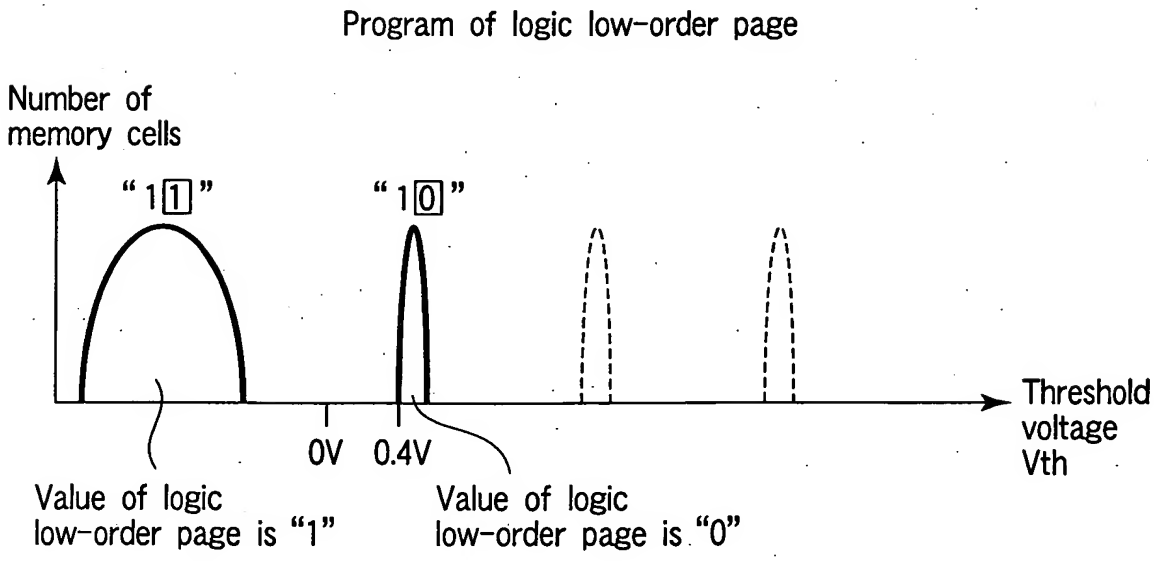

Program of logic low-order page
Number of memory cells
"11"
"10"
Threshold voltage Vth
0V
0.4V
Value of logic low-order page is "1"
Value of logic low-order page is "0"

FIG. 18

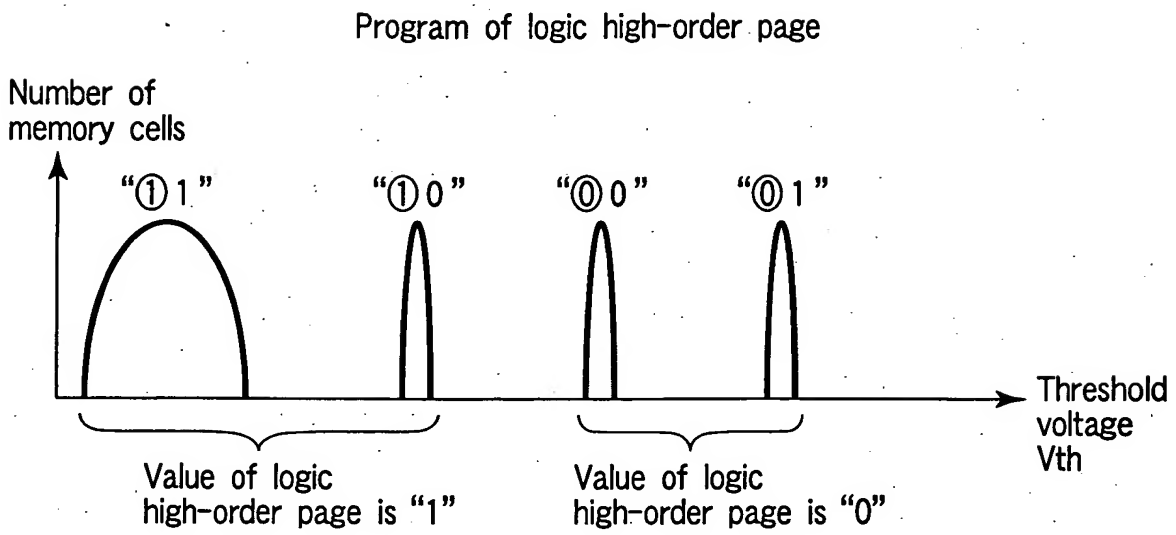

Program of logic high-order page
Number of memory cells
"① 1"
"① 0"
"⓪ 0"
"⓪ 1"
Threshold voltage Vth
Value of logic high-order page is "1"
Value of logic high-order page is "0"

FIG. 19

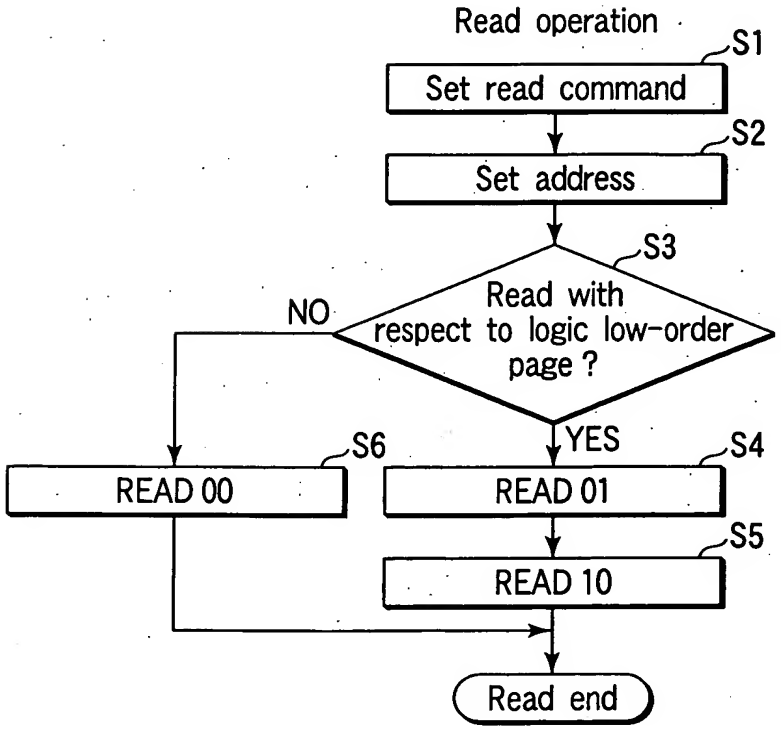

Read operation
S1
Set read command
S2
Set address
S3
Read with respect to logic low-order page ?
NO
YES
S6
READ 00
S4
READ 01
S5
READ 10
Read end

FIG. 20

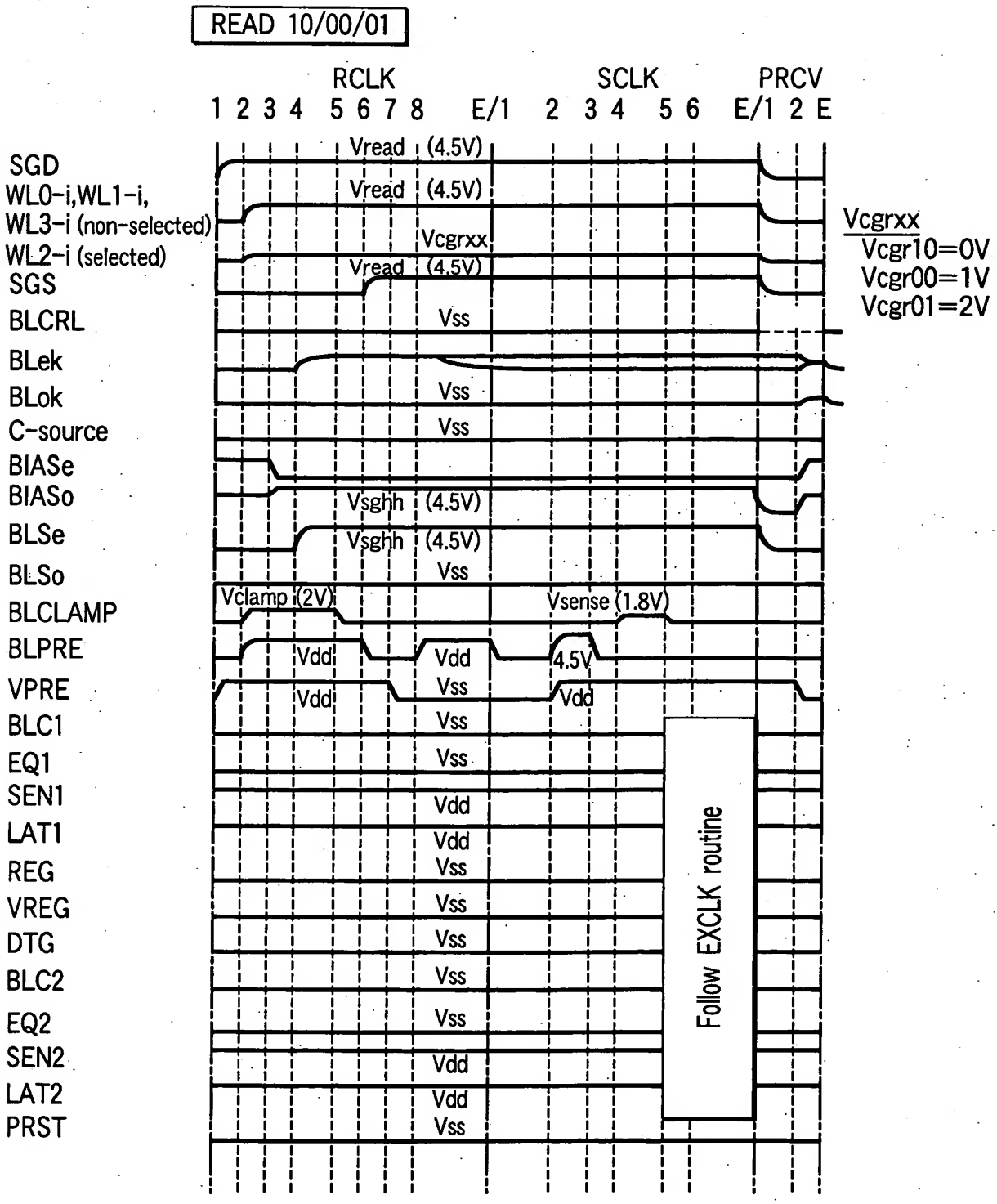
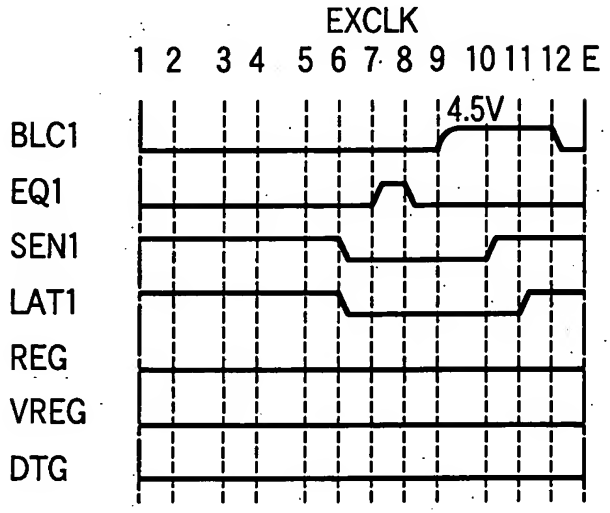

READ 10/00/01
RCLK
SCLK
PRCV
1 2 3 4 5 6 7 8 E/1 2 3 4 5 6 E/1 2 E
SGD
WL0-i,WL1-i,
WL3-i (non-selected)
WL2-i (selected)
SGS
BLCRL
BLek
BLok
C-source
BIASe
BIASo
BLSe
BLSo
BLCLAMP
BLPRE
VPRE
BLC1
EQ1
SEN1
LAT1
REG
VREG
DTG
BLC2
EQ2
SEN2
LAT2
PRST
Vread (4.5V)
Vcgrxx
Vss
Vsghh (4.5V)
Vclamp (2V)
Vsense (1.8V)
Vdd
4.5V
Follow EXCLK routine
Vcgrxx
Vcgr10=0V
Vcgr00=1V
Vcgr01=2V

FIG. 21

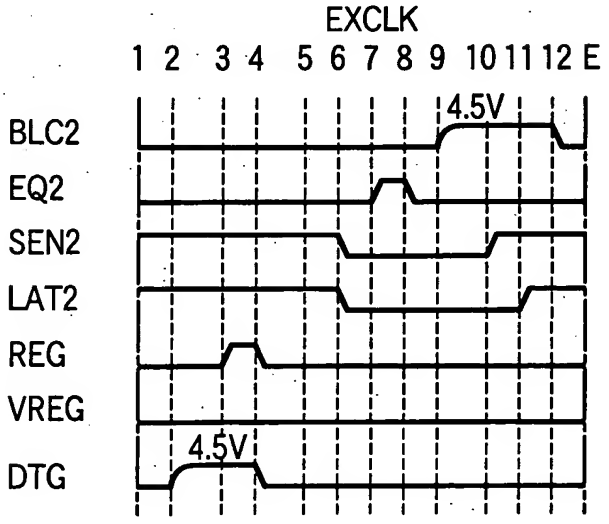
READ01 (EXCLK routine)



No change in signals other than shown signals

FIG. 22

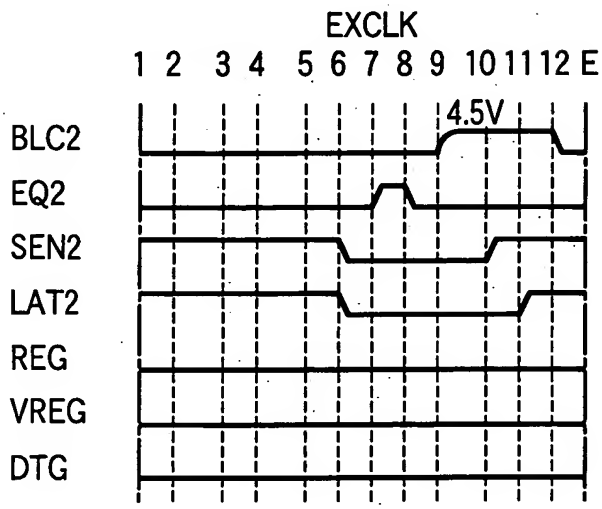
READ10 (EXCLK routine)



No change in signals other than shown signals

FIG. 23

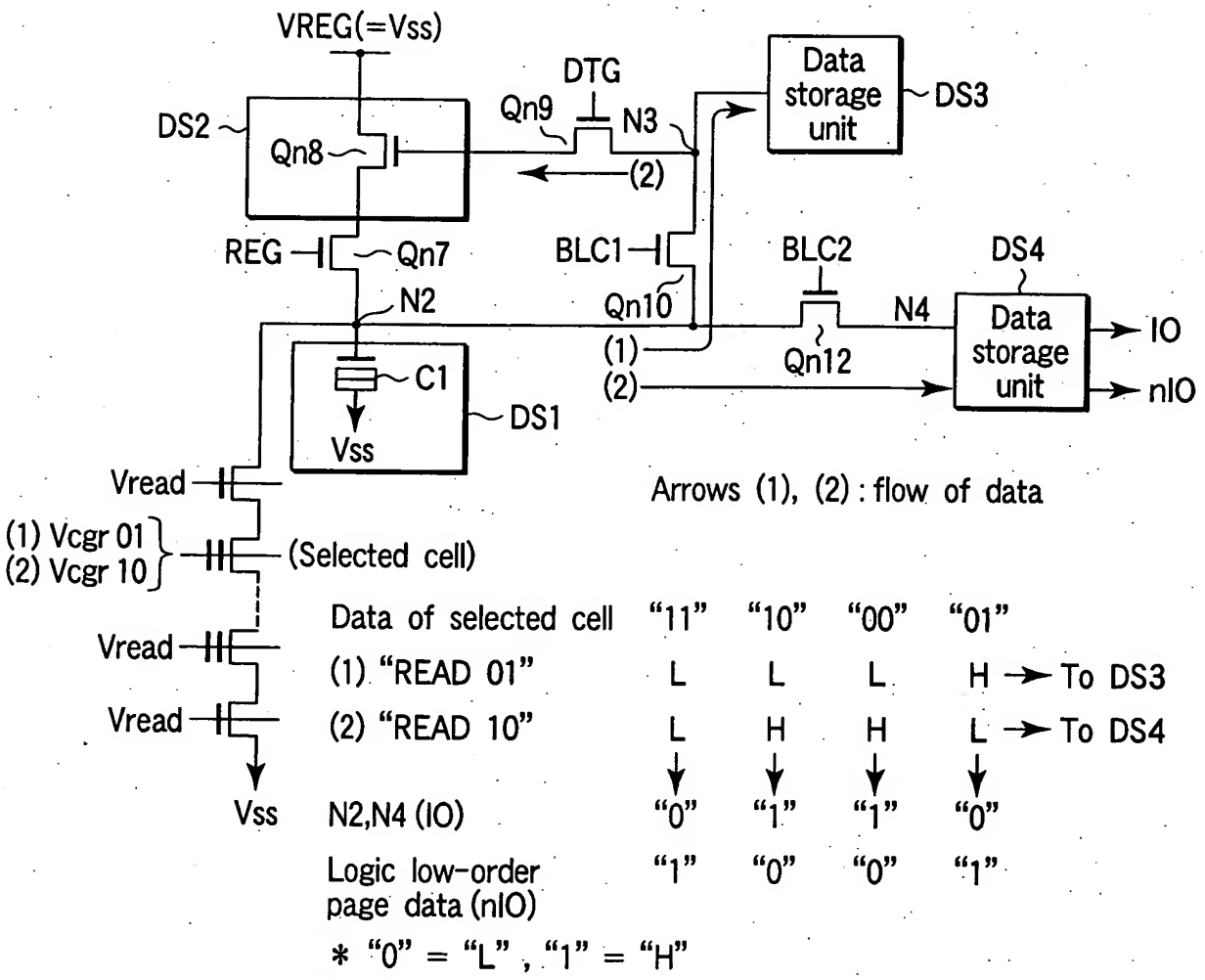
READ00 (EXCLK routine)



No change in signals other than shown signals

FIG. 24

Read of logic low-order page data

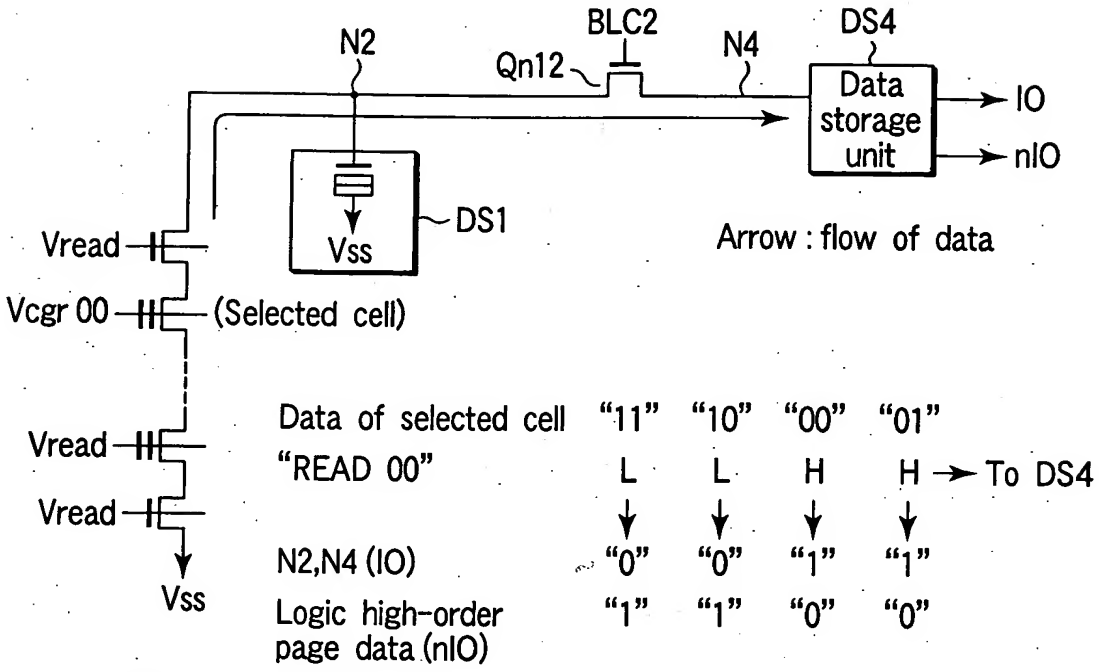


Data of selected cell	"11"	"10"	"00"	"01"	
(1) "READ 01"	L	L	L	H	→ To DS3
(2) "READ 10"	L	H	H	L	→ To DS4
N2,N4 (IO)	"0"	"1"	"1"	"0"	
Logic low-order page data (nIO)	"1"	"0"	"0"	"1"	

* "0" = "L", "1" = "H"

FIG. 25

Read of logic high-order page data



Data of selected cell	"11"	"10"	"00"	"01"	
"READ 00"	L	L	H	H	→ To DS4
	↓	↓	↓	↓	
N2,N4 (IO)	"0"	"0"	"1"	"1"	
Logic high-order page data (nIO)	"1"	"1"	"0"	"0"	

* "0" = "L" , "1" = "H"

FIG. 26

Program operation 1 (Pass Write)

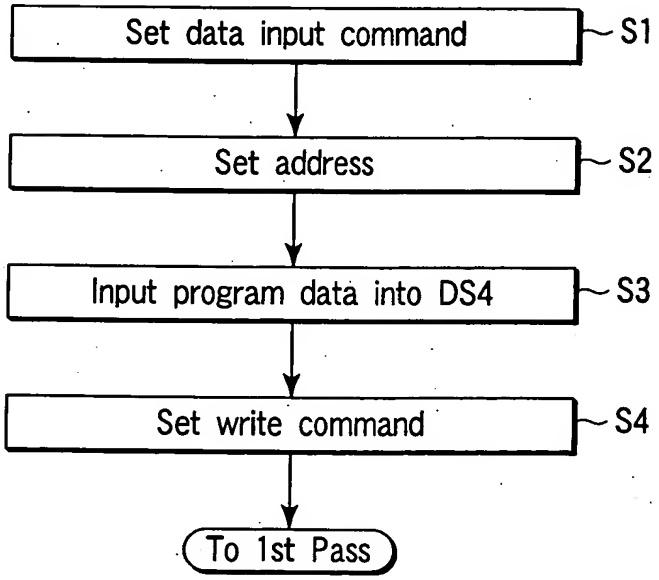


FIG. 27

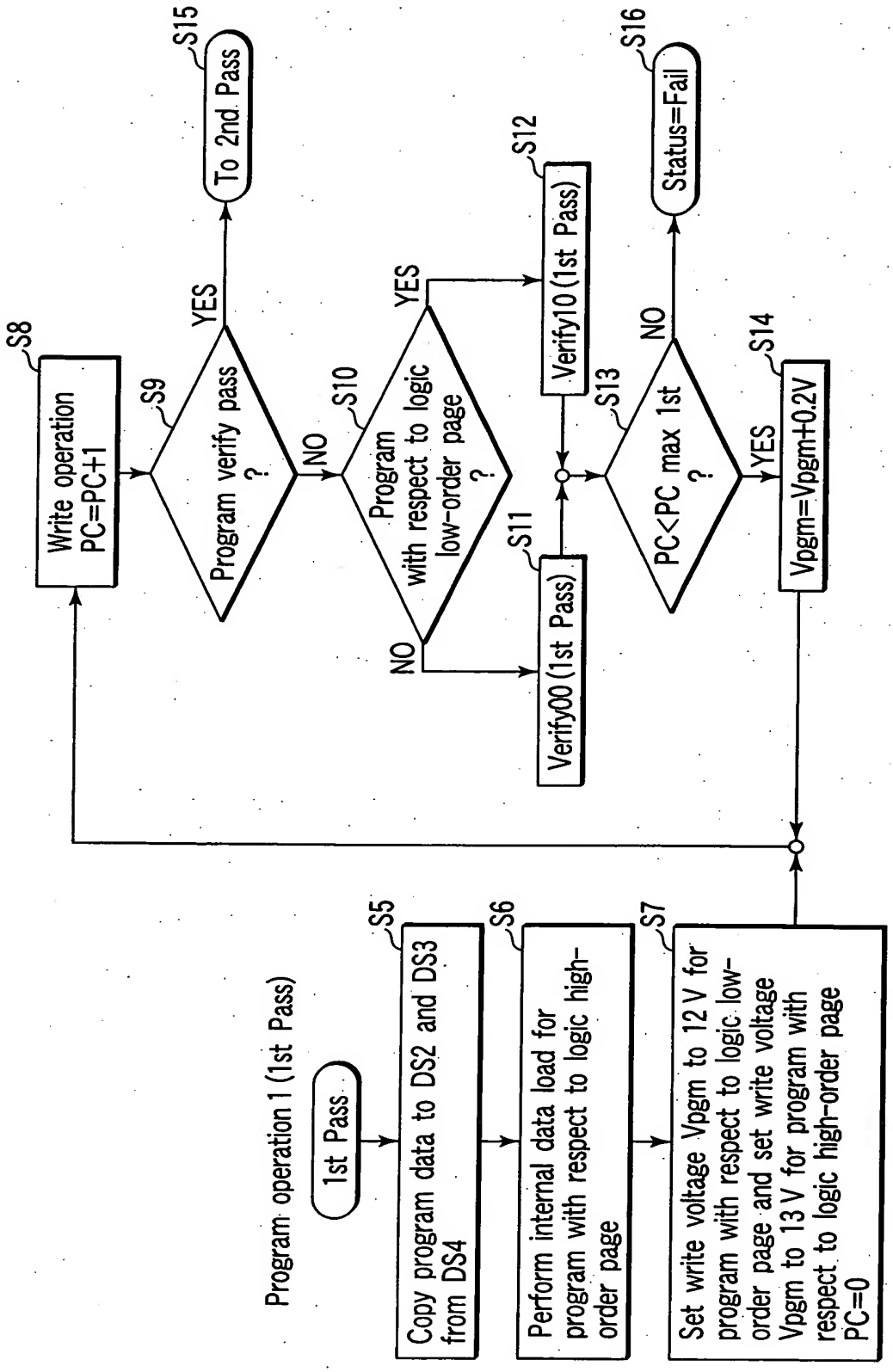

Program operation 1 (1st Pass)
1st Pass
S5
Copy program data to DS2 and DS3 from DS4
S6
Perform internal data load for program with respect to logic high-order page
S7
Set write voltage Vpgm to 12 V for program with respect to logic low-order page and set write voltage Vpgm to 13 V for program with respect to logic high-order page PC=0
S8
Write operation PC=PC+1
S9
Program verify pass ?
YES
S15
To 2nd Pass
NO
S10
Program with respect to logic low-order page ?
YES
S12
Verify10 (1st Pass)
NO
S11
Verify00 (1st Pass)
S13
PC<PC max 1st ?
NO
S16
Status=Fail
YES
S14
Vpgm=Vpgm+0.2V

FIG. 28

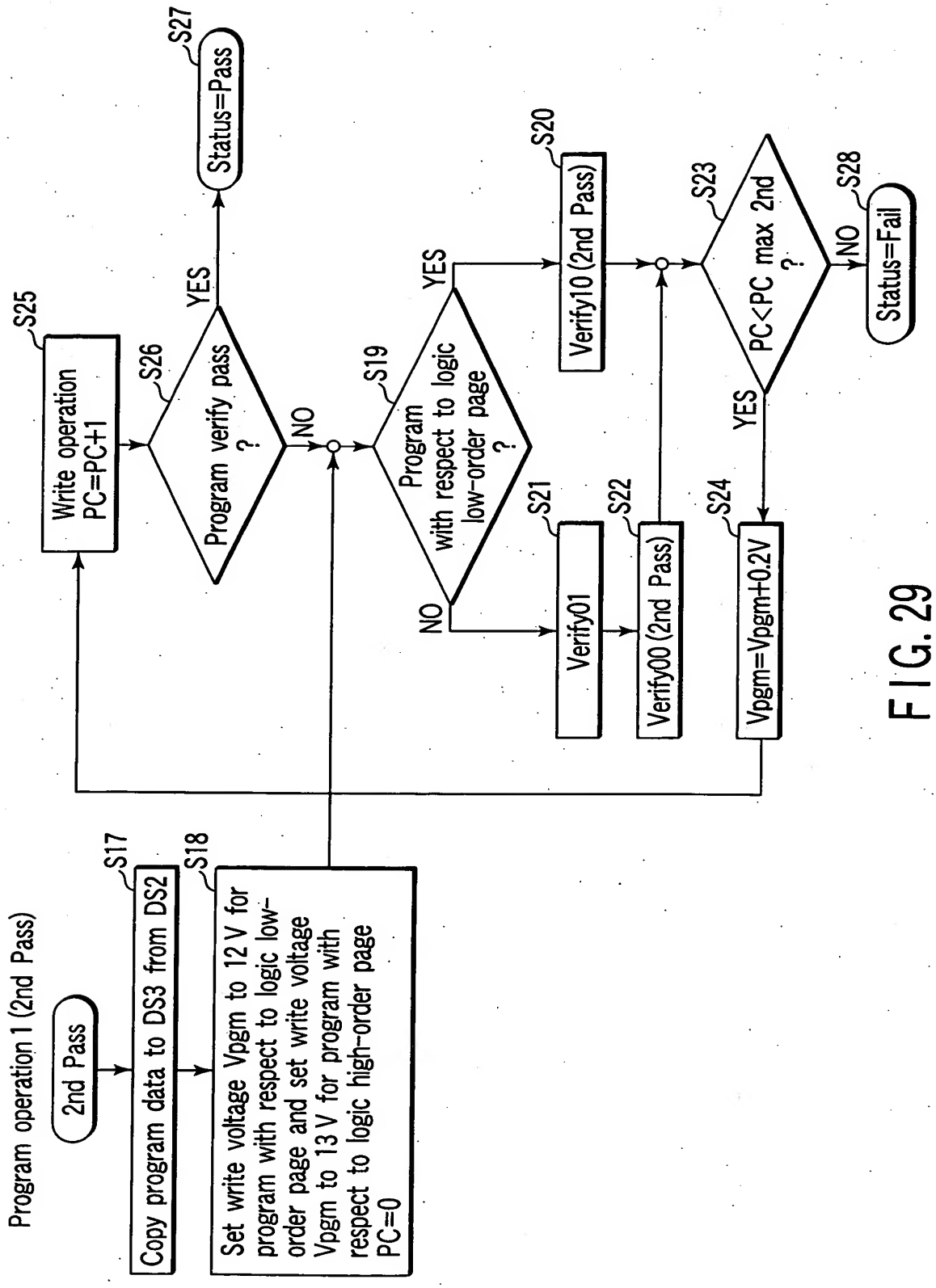

Program operation 1 (2nd Pass)
2nd Pass
S17
Copy program data to DS3 from DS2
S18
Set write voltage Vpgm to 12 V for program with respect to logic low-order page and set write voltage Vpgm to 13 V for program with respect to logic high-order page PC=0
S25
Write operation PC=PC+1
S26
Program verify pass ?
YES
S27
Status=Pass
NO
S19
Program with respect to logic low-order page ?
YES
S20
Verify10 (2nd Pass)
NO
S21
Verify01
S22
Verify00 (2nd Pass)
S23
PC<PC max 2nd ?
YES
S24
Vpgm=Vpgm+0.2V
NO
S28
Status=Fail

FIG. 29

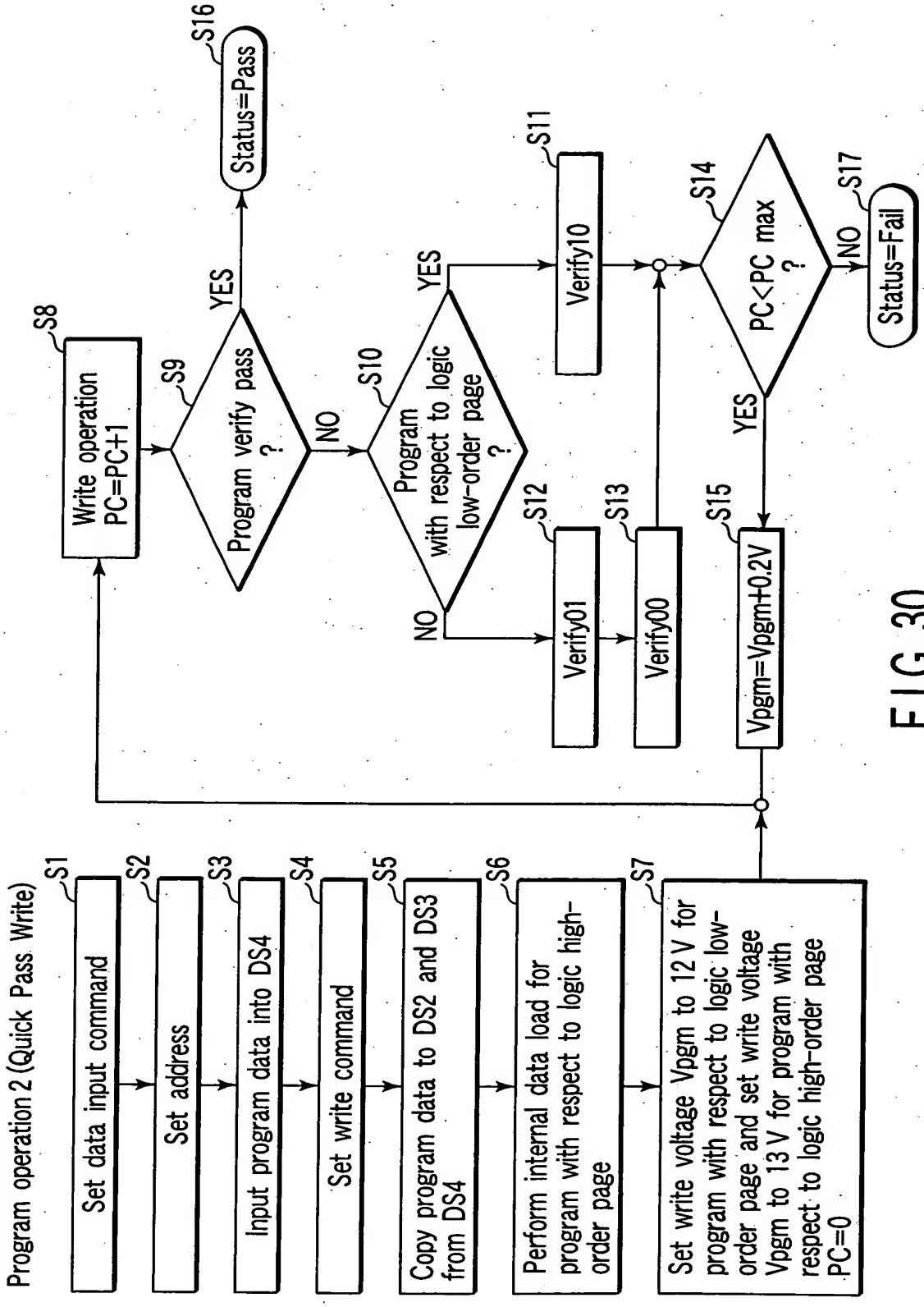

Program operation 2 (Quick Pass Write)
S1
Set data input command
S2
Set address
S3
Input program data into DS4
S4
Set write command
S5
Copy program data to DS2 and DS3 from DS4
S6
Perform internal data load for program with respect to logic high-order page
S7
Set write voltage Vpgm to 12 V for program with respect to logic low-order page and set write voltage Vpgm to 13 V for program with respect to logic high-order page PC=0
S8
Write operation PC=PC+1
S9
Program verify pass ?
YES
S16
Status=Pass
NO
S10
Program with respect to logic low-order page ?
YES
S11
Verify10
NO
S12
Verify01
S13
Verify00
S14
PC<PC max ?
YES
S15
Vpgm=Vpgm+0.2V
NO
S17
Status=Fail

FIG. 30

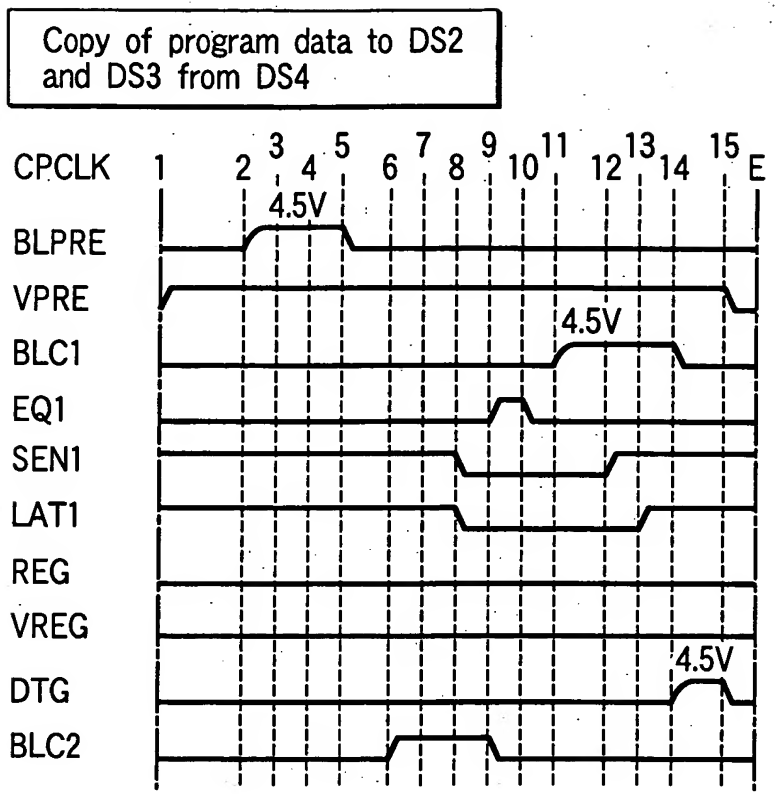

Copy of program data to DS2 and DS3 from DS4
CPCLK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
E
4.5V
BLPRE
VPRE
4.5V
BLC1
EQ1
SEN1
LAT1
REG
VREG
4.5V
DTG
BLC2

FIG. 31

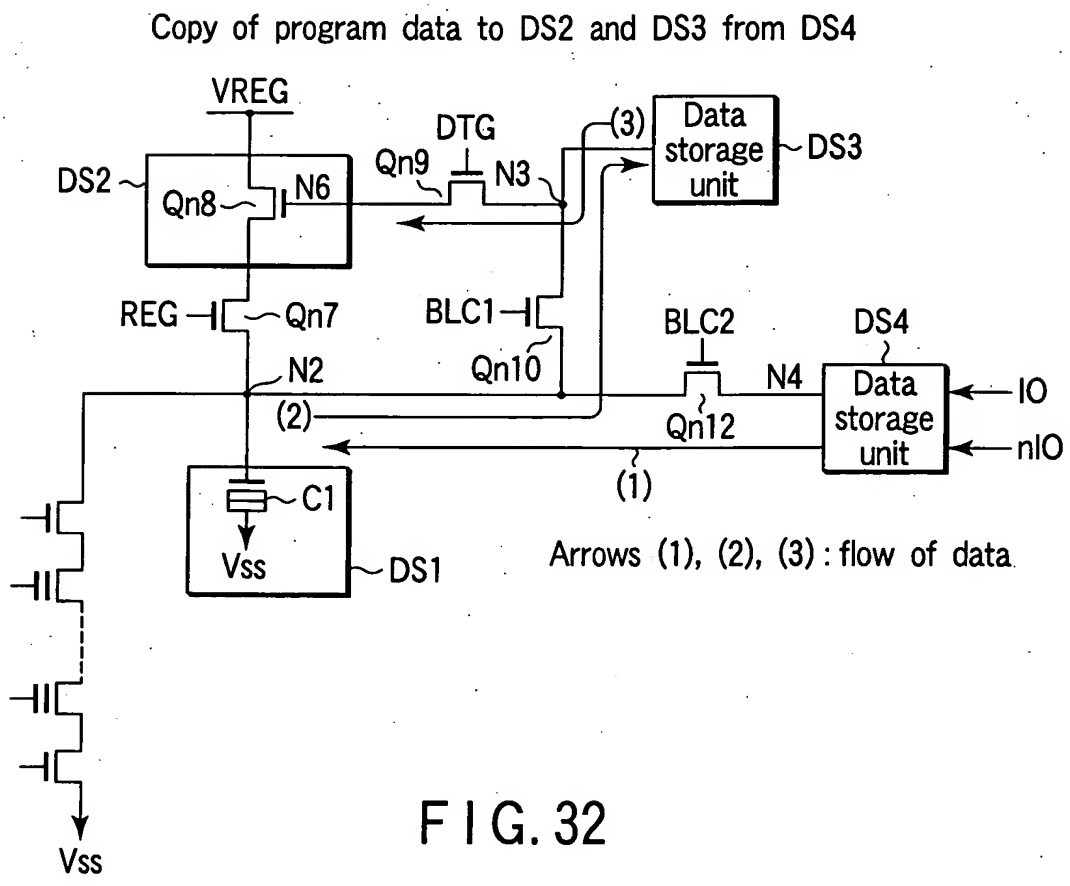

Copy of program data to DS2 and DS3 from DS4
VREG
DTG
(3)
Data storage unit
DS3
DS2
Qn8
N6
Qn9
N3
REG
Qn7
BLC1
Qn10
BLC2
DS4
N2
N4
Data storage unit
IO
nIO
(2)
Qn12
(1)
C1
Vss
DS1
Arrows (1), (2), (3) : flow of data
Vss

FIG. 32

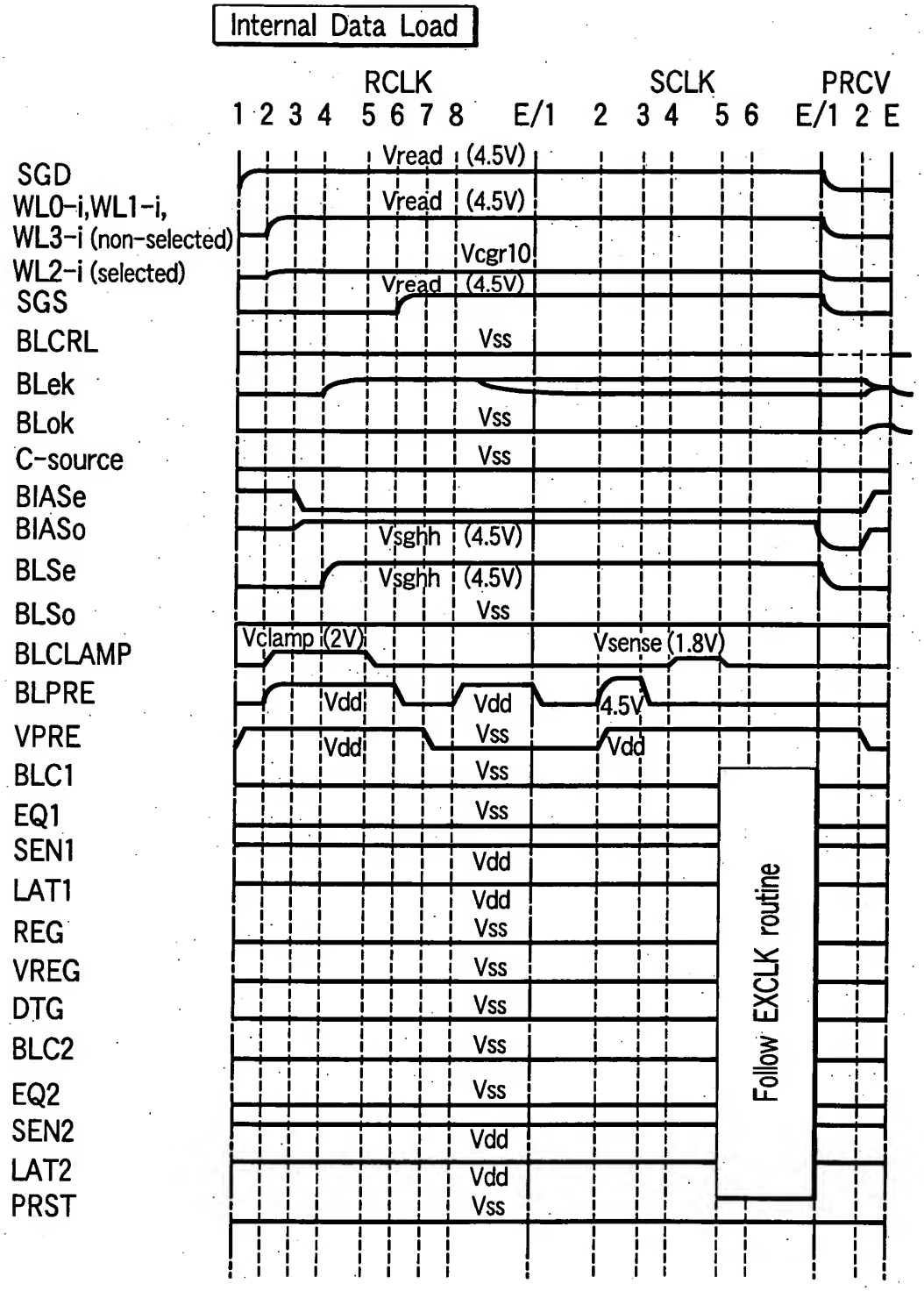

Internal Data Load
RCLK
SCLK
PRCV
1 2 3 4 5 6 7 8 E/1 2 3 4 5 6 E/1 2 E
SGD
WL0-i,WL1-i,
WL3-i (non-selected)
WL2-i (selected)
SGS
BLCRL
BLek
BLok
C-source
BIASe
BIASo
BLSe
BLSo
BLCLAMP
BLPRE
VPRE
BLC1
EQ1
SEN1
LAT1
REG
VREG
DTG
BLC2
EQ2
SEN2
LAT2
PRST
Vread (4.5V)
Vcgr10
Vss
Vsghh (4.5V)
Vclamp (2V)
Vsense (1.8V)
Vdd
4.5V
Follow EXCLK routine

FIG. 33

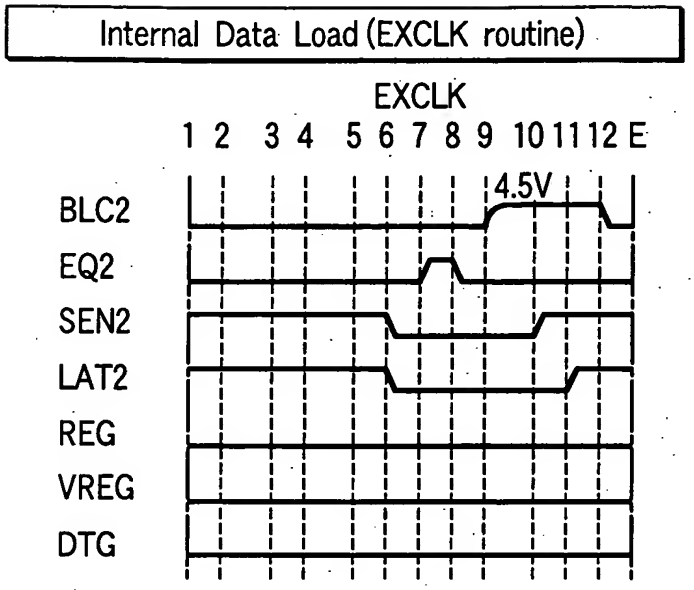


FIG. 34 No change in signals other than shown signals

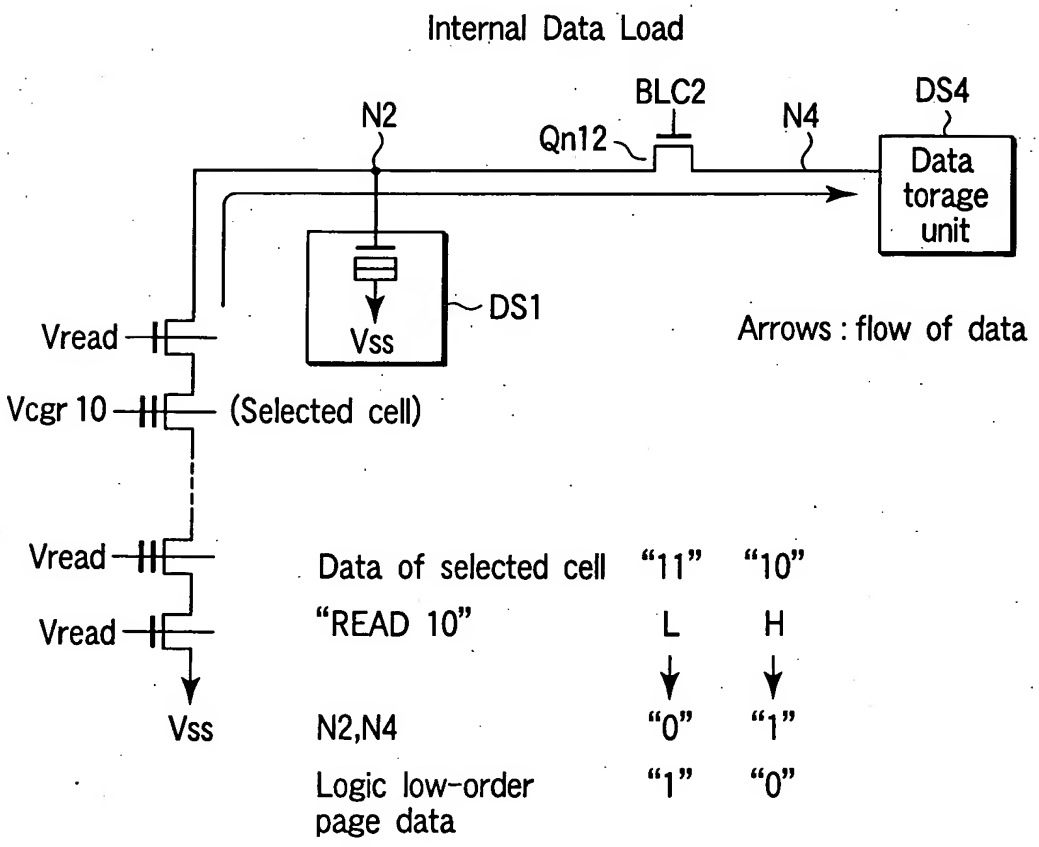


FIG. 35 * "0" = "L", "1" = "H"

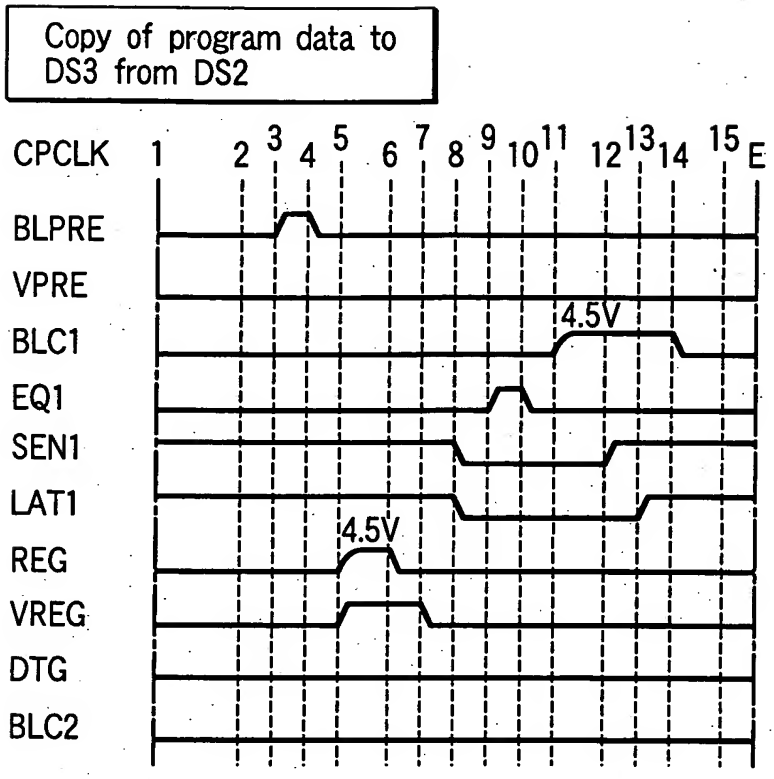

Copy of program data to DS3 from DS2
CPCLK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
E
BLPRE
VPRE
BLC1
EQ1
SEN1
LAT1
REG
VREG
DTG
BLC2
4.5V
4.5V

FIG. 36

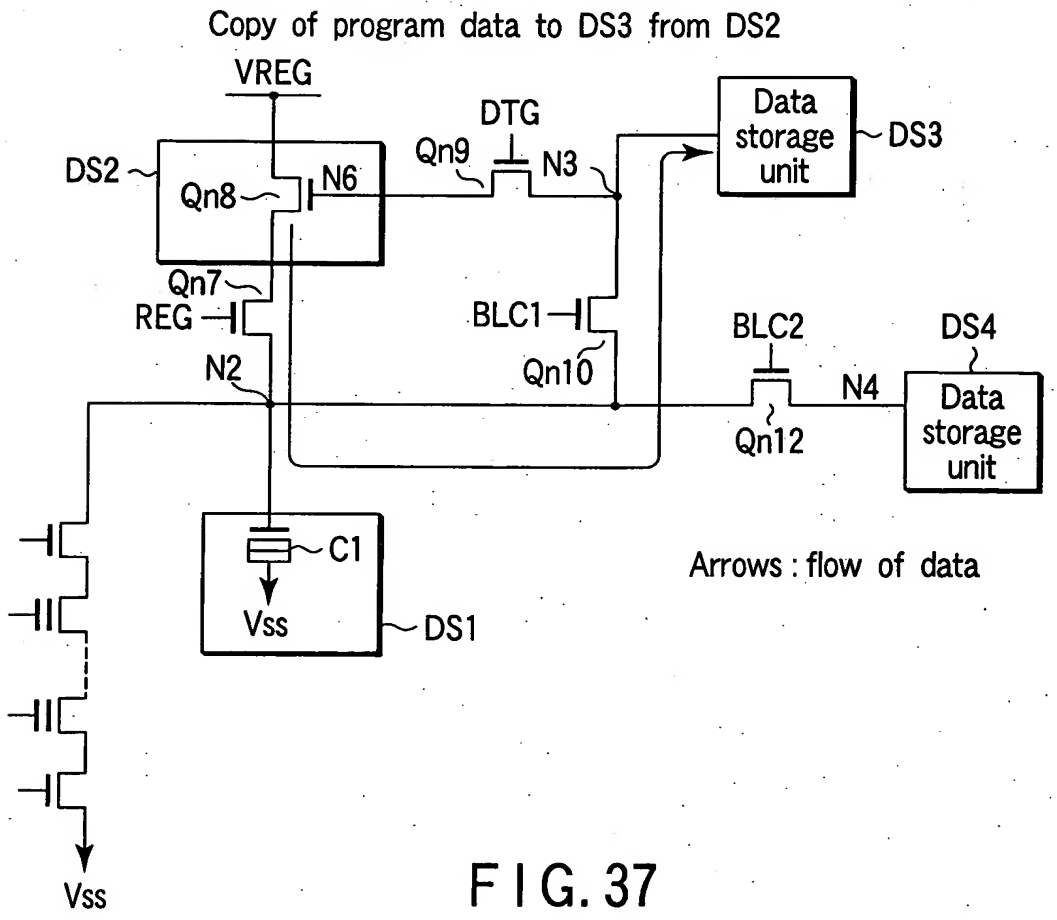

Copy of program data to DS3 from DS2
VREG
DTG
Data storage unit
DS3
DS2
Qn8
N6
Qn9
N3
Qn7
REG
N2
BLC1
Qn10
BLC2
Qn12
N4
DS4
Data storage unit
C1
Vss
DS1
Arrows : flow of data
Vss

FIG. 37

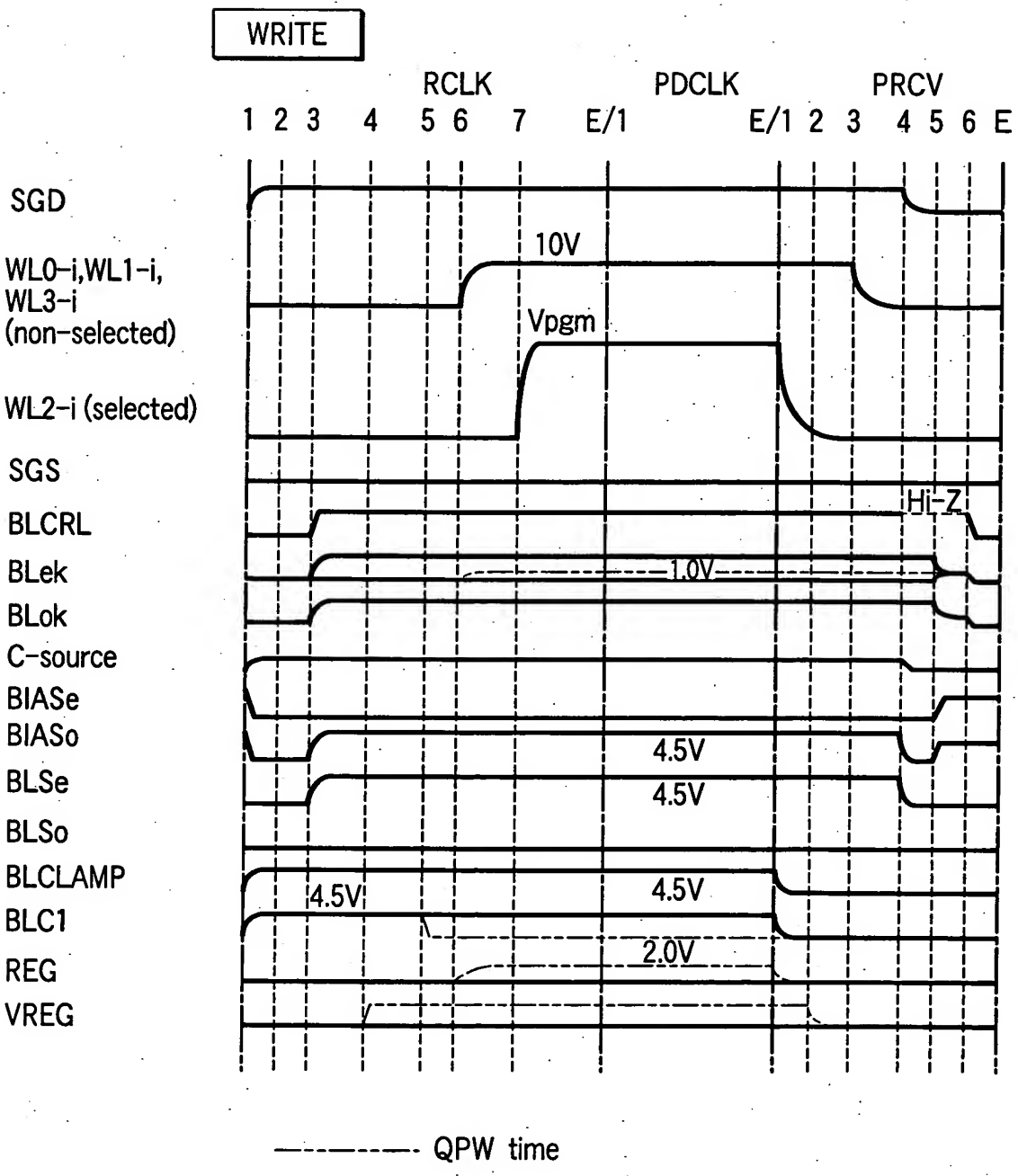

WRITE
RCLK
PDCLK
PRCV
1 2 3 4 5 6 7 E/1 E/1 2 3 4 5 6 E
SGD
WL0-i,WL1-i,
WL3-i
(non-selected)
WL2-i (selected)
SGS
BLCRL
BLek
BLok
C-source
BIASe
BIASo
BLSe
BLSo
BLCLAMP
BLC1
REG
VREG
10V
Vpgm
Hi-Z
1.0V
4.5V
4.5V
4.5V
4.5V
2.0V
QPW time

FIG. 38

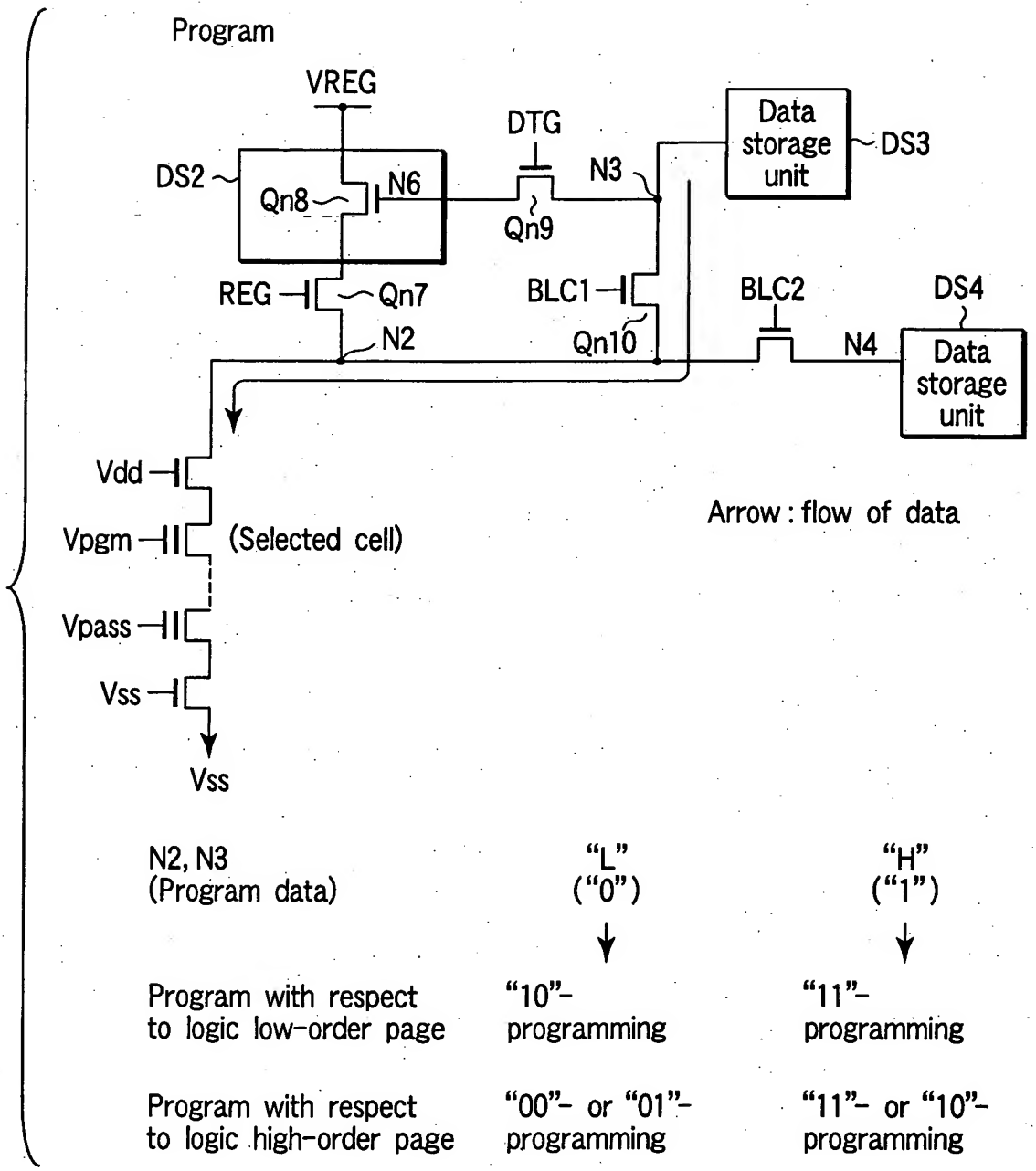

Program
VREG
DTG
Data storage unit
DS3
DS2
Qn8
N6
N3
Qn9
REG
Qn7
BLC1
BLC2
DS4
N2
Qn10
N4
Data storage unit
Vdd
Arrow : flow of data
Vpgm
(Selected cell)
Vpass
Vss
Vss
N2, N3 (Program data)
"L" ("0")
"H" ("1")
Program with respect to logic low-order page
"10"- programming
"11"- programming
Program with respect to logic high-order page
"00"- or "01"- programming
"11"- or "10"- programming

FIG. 39

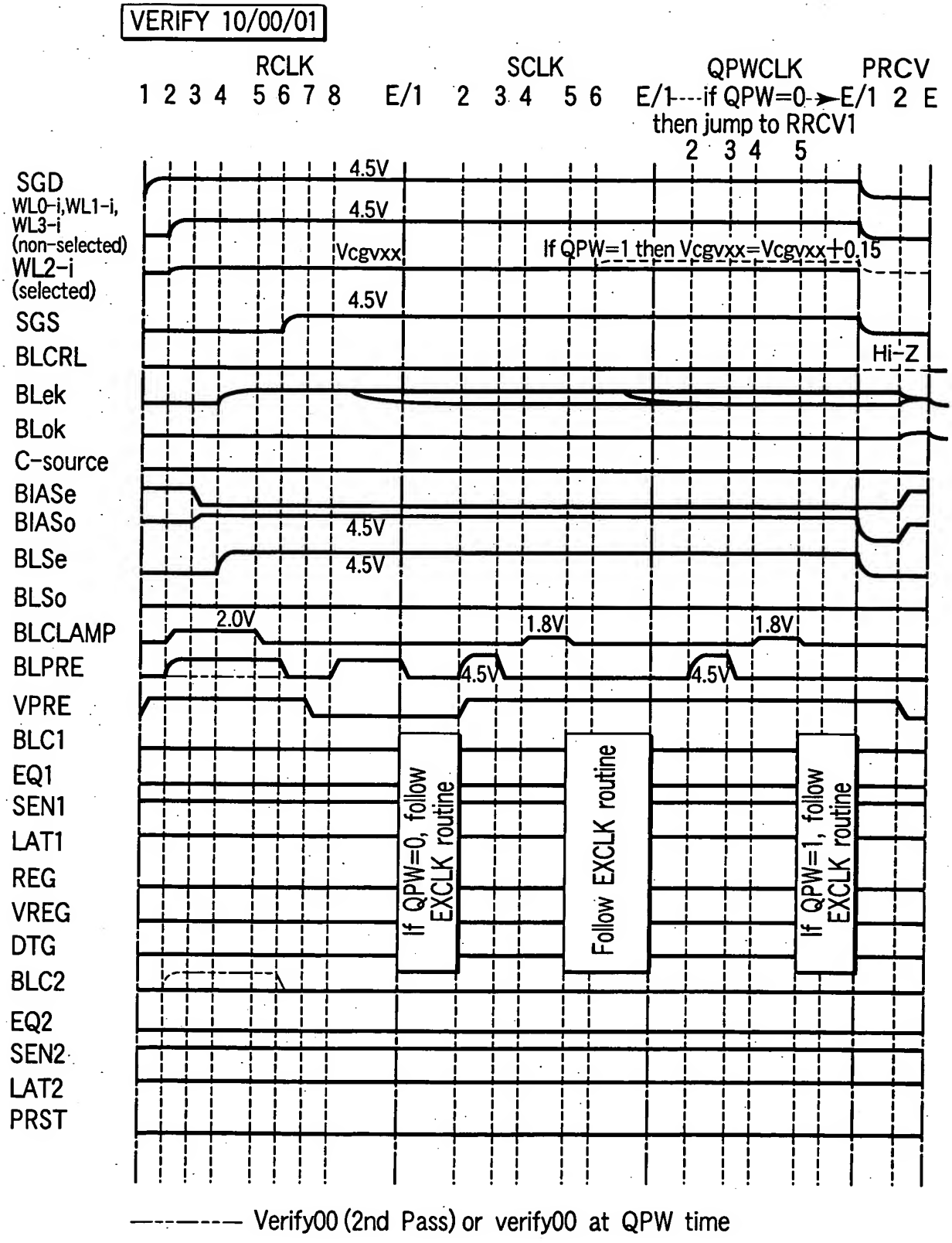
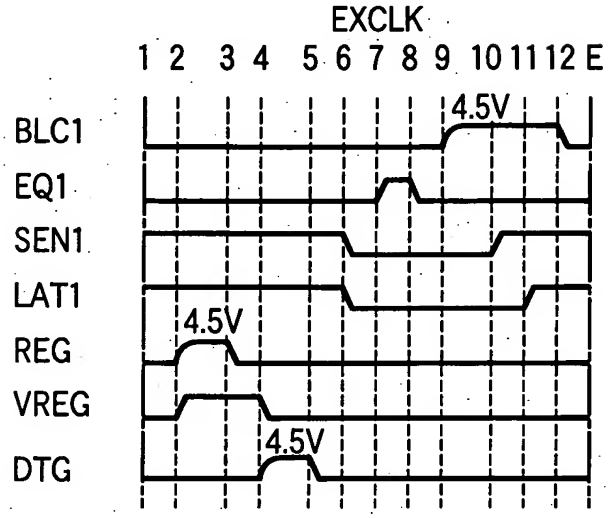

VERIFY 10/00/01
RCLK
1 2 3 4 5 6 7 8
SCLK
E/1 2 3 4 5 6
QPWCLK
E/1---if QPW=0→E/1 2 E
then jump to RRCV1
2 3 4 5
PRCV
1 2 E
SGD
WL0-i,WL1-i,
WL3-i
(non-selected)
WL2-i
(selected)
SGS
BLCRL
BLek
BLok
C-source
BIASe
BIASo
BLSe
BLSo
BLCLAMP
BLPRE
VPRE
BLC1
EQ1
SEN1
LAT1
REG
VREG
DTG
BLC2
EQ2
SEN2
LAT2
PRST
4.5V
Vcgvxx
If QPW=1 then Vcgvxx=Vcgvxx+0.15
Hi-Z
2.0V
1.8V
If QPW=0, follow EXCLK routine
Follow EXCLK routine
If QPW=1, follow EXCLK routine
Verify00 (2nd Pass) or verify00 at QPW time

FIG. 40

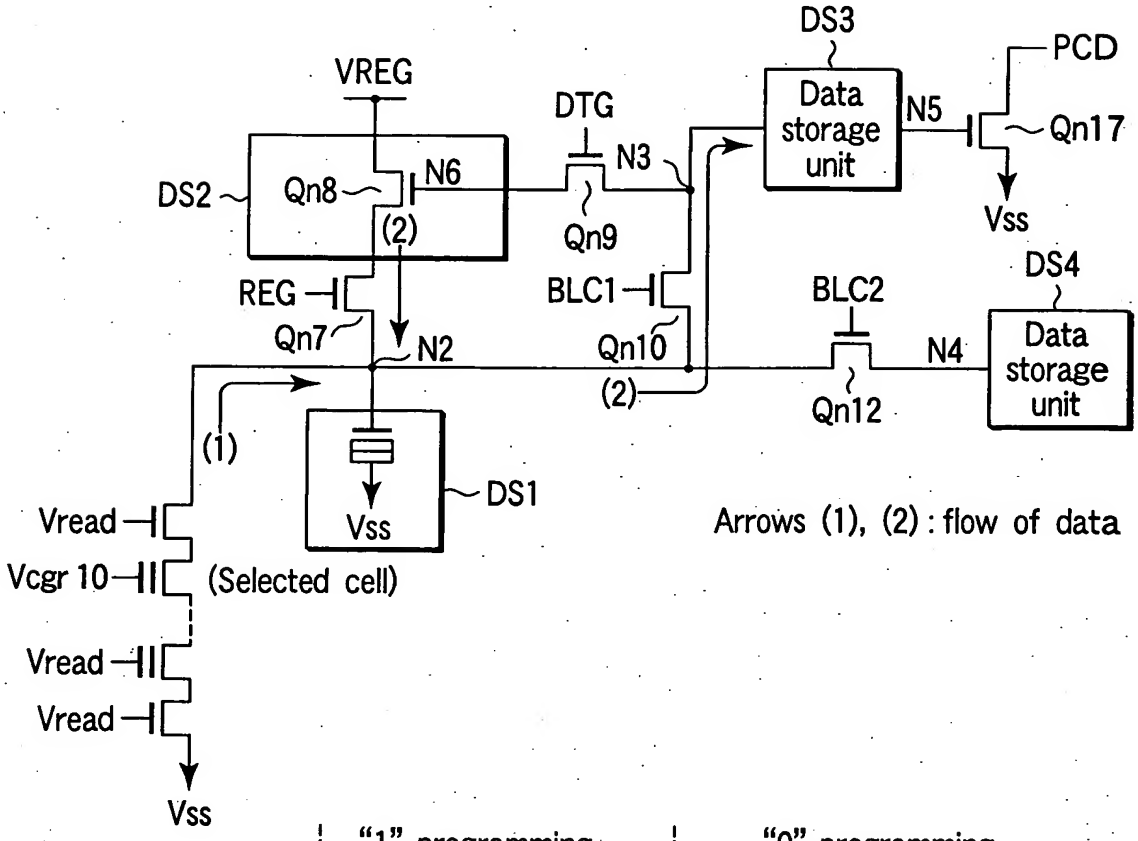
VERIFY10/VERIFY00/VERIFY01
(EXCLK routine)



No change in signals other than shown signals

FIG. 41

Program with respect to logic low-order page
"VERIFY 10" + "COMPLETION DETECTION"

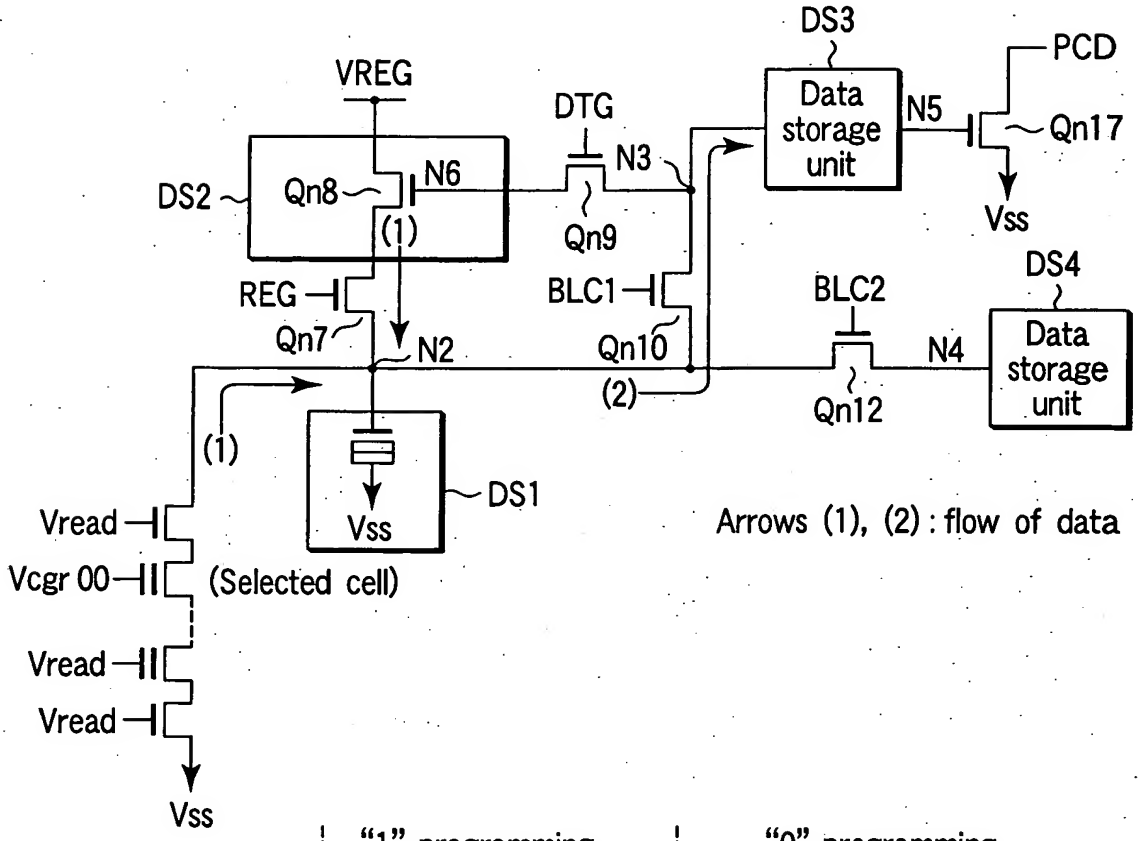


	"1"-programming		"0"-programming	
Data of selected cell (present state)	"11"		"11"	"10"
(1) DS1(N2)	"L" ("0") ⇨	"H" ("1")	"L" ("0")	"H" ("1")
(1) DS2(N6) Program data	"H" ("1")	※Forcibly set DS1 to "H"	"L" ("0")	"L" ("0")
(2) DS3(N3)	"H" ("1")		"L" ("0")	"H" ("1")
N5	"L" program completed		"H" program uncompleted	"L" program completed

※ "Verify 10" includes "verify 10 (1st Pass)" in Write Pass, "Verify 10 (2nd Pass)" and "Verify 10" in Qwp

FIG. 42

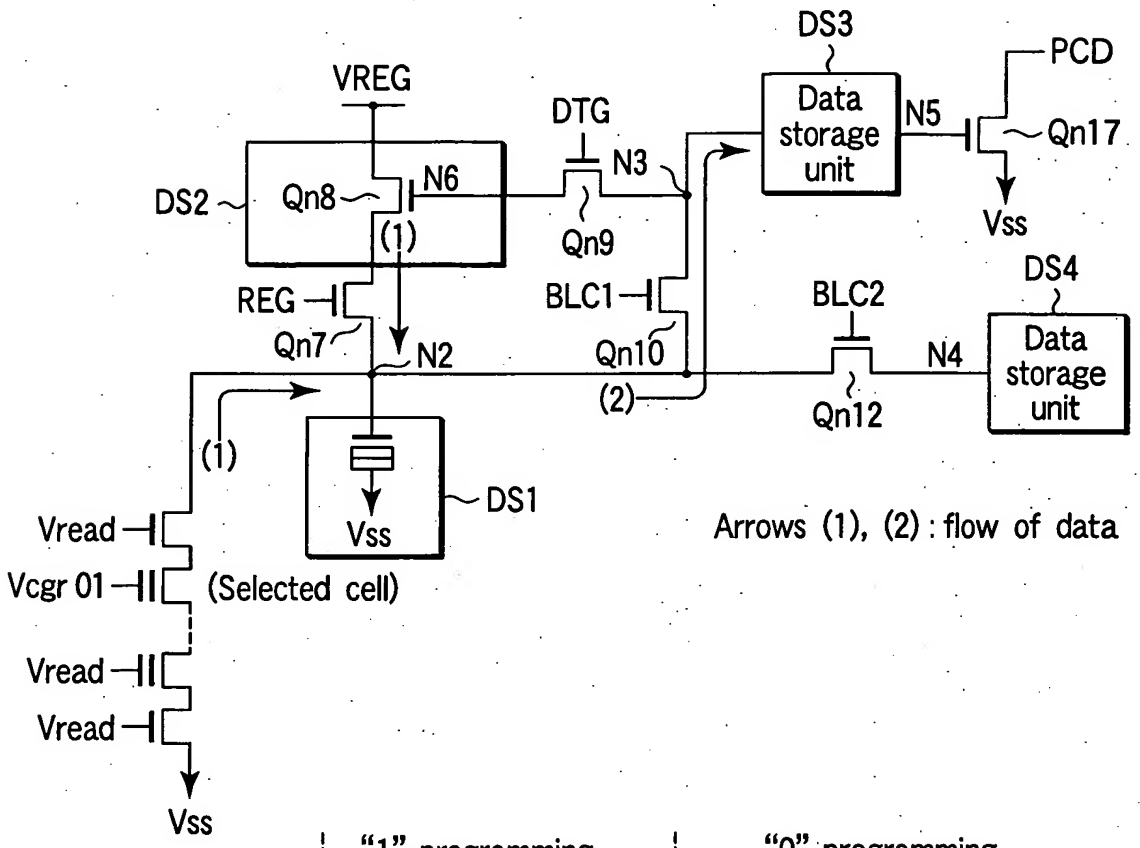
Program with respect to logic high-order page
"VERIFY 00 (1st Pass)" + "COMPLETION DETECTION"



	"1"-programming		"0"-programming	
Data of selected cell (present state)	"11" or "10"		"11" or "10"	"00"
(1) DS1(N2)	"L" ("0") ⇨	"H" ("1")	"L" ("0")	"H" ("1")
(1) DS2(N6) Program data	"H" ("1")	※Forcibly set DS1 to "H"	"L" ("0")	"L" ("0")
(2) DS3(N3)	"H" ("1")		"L" ("0")	"H" ("1")
N5	"L" program completed		"H" program uncompleted	"L" program completed

FIG. 43

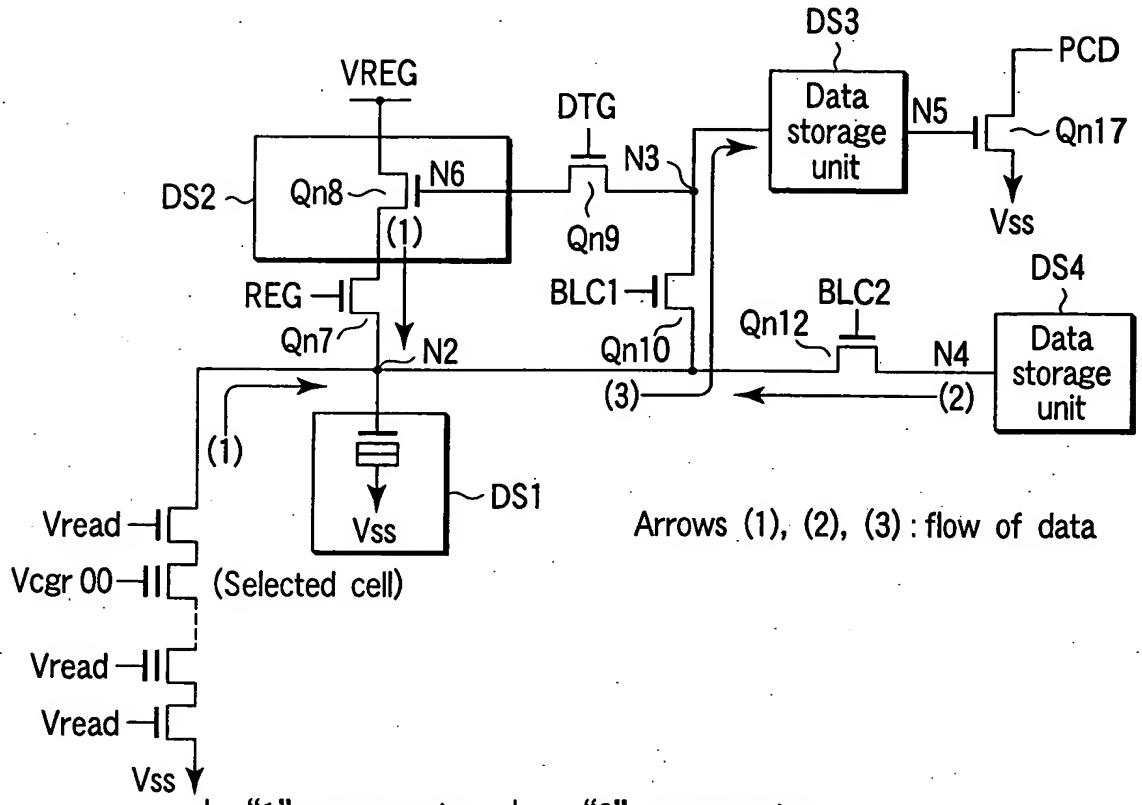
Program with respect to logic high-order page
"VERIFY 01" + "COMPLETION DETECTION"



	"1"-programming		"0"-programming	
Data of selected cell (present state)	"11" or "10"		"11" or "10" or "00"	"01"
(1) DS1(N2)	"L" ("0") ⇨	"H" ("1")	"L" ("0")	"H" ("1")
(1) DS2(N6) Program data	"H" ("1")	※Forcibly set DS1 to "H"	"L" ("0")	"L" ("0")
(2) DS3(N3)	"H" ("1")		"L" ("0")	"H" ("1")
N5	"L" program completed		"H" program uncompleted	"L" program completed

FIG. 44

Program with respect to logic high-order page
"VERIFY 00 (2nd Pass)" + "COMPLETION DETECTION"



	"1"-programming		"0"-programming		
Data of selected cell (present state)	"11" or "10"		"11" or "10"	"00"	
(1) DS1(N2)	"L" ("0") ⇨ "H" ("1")		"L" ("0")	"H" ("1")	
(2) DS2(N6) Program data	"H" ("1")	※Forcibly set DS1 to "H"	"L" ("0")	"L" ("0")	
(2) Logic low-order page data (N4)				"0" ("H")	"1" ("L") ※Forcibly set DS1 to "L"
				"00"-programing	"01"-programing
(2) DS1(N2)				"H" ("1")	"H" ("1") ⇨ "L" ("0")
(3) DS3(N3)	"H" ("1")		"L" ("0")	"H" ("1")	"L" ("0")
N5	"L" program completed		"H" program uncompleted	"L" program completed	"H" program uncompleted

FIG. 45